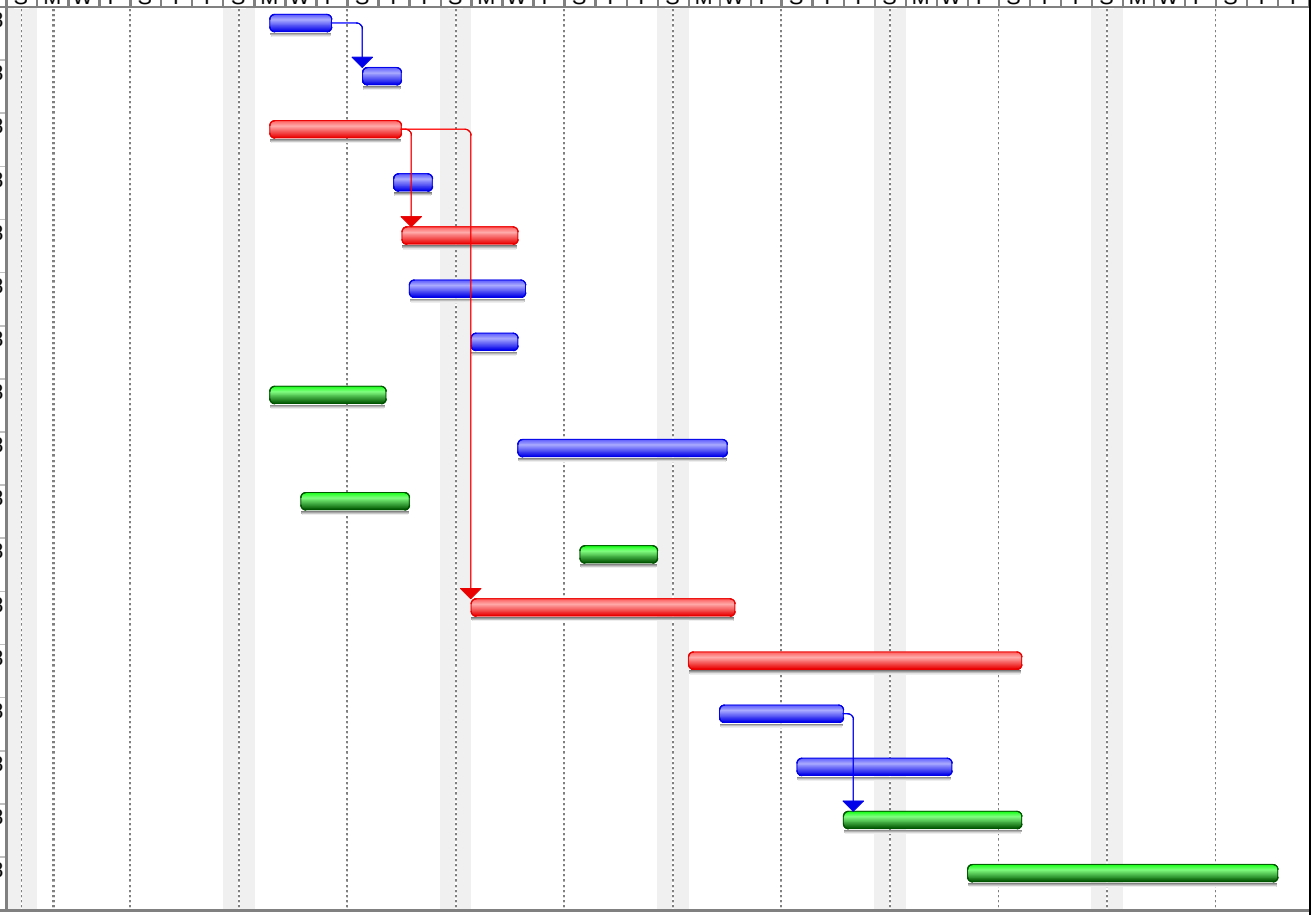
ID	Task Name	Duration	Start
1	Build all unary gates in lab	0.8 wks?	/1/08
2	Build 3 x 3:1 multiplexers	2.5 days?	/7/08
3	Expression evaluator working	1.3 wks?	/1/08
4	Build dyadic gates in lab	0.5 wks?	/9/08
5	Instruction-level simulator working	5.5 days?	/9/08
6	Build 9-trit SWROM	5.5 days?	10/08
7	Build ternary cycling gate, connect to SWR(	3 days?	14/08
8	Administrative tasks	5.5 days?	/1/08
9	Build tri-flop circuits	9.5 days?	17/08
10	Simulate all tri-flop circuits	5 days?	/3/08
11	Evaluate progress	5 days?	21/08
12	Enhance expr. eval.; generate circuits, GUI	13 days?	14/08
13	High-level language to asm compiler	15.5 days?	28/08
14	Design and build ALU	6 days?	30/08
15	Design and build instruction decoder	8 days?	/5/08
16	Integration	7.5 days?	/8/08
17	Finishing touches or catch up	14 days?	16/08



Project: Spring 2008 Schedule
Date: Tue 3/18/08

Task
Split
Progress
Milestone
Summary
Project Summary
External Tasks
External Milestone
Deadline