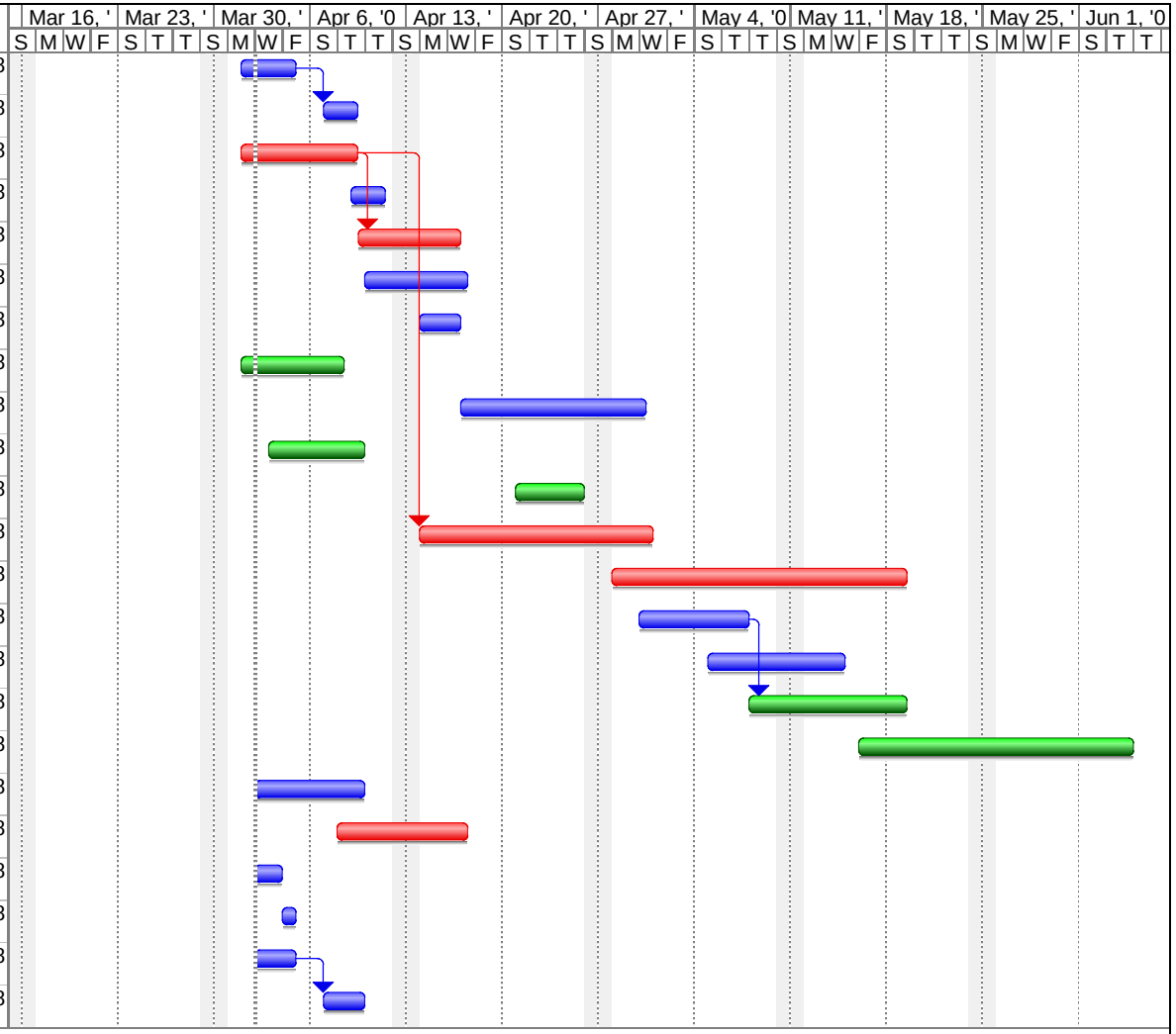
ID	Task Name	Duration	Start	Finish
1	Build all unary gates in lab	0.8 wks?	Tue 4/1/08	ri 4/4/08
2	Build 3 x 3:1 multiplexers	2.5 days?	Mon 4/7/08	d 4/9/08
3	Expression evaluator working	1.3 wks?	Tue 4/1/08	d 4/9/08
4	Build dyadic gates in lab	0.5 wks?	Wed 4/9/08	4/11/08
5	Instruction-level simulator working	5.5 days?	Wed 4/9/08	4/16/08
6	Build 9-trit SWROM	5.5 days?	hu 4/10/08	4/17/08
7	Build ternary cycling gate, connect to SWR	3 days?	on 4/14/08	4/16/08
8	Administrative tasks	5.5 days?	Tue 4/1/08	e 4/8/08
9	Build tri-flop circuits	9.5 days?	hu 4/17/08	4/30/08
10	Simulate all tri-flop circuits	5 days?	Thu 4/3/08	d 4/9/08
11	Evaluate progress	5 days?	on 4/21/08	4/25/08
12	Enhance expr. eval.; generate circuits, GUI	13 days?	on 4/14/08	4/30/08
13	High-level language to asm compiler	15.5 days?	on 4/28/08	5/19/08
14	Design and build ALU	6 days?	ed 4/30/08	d 5/7/08
15	Design and build instruction decoder	8 days?	Mon 5/5/08	5/14/08
16	Integration	7.5 days?	Thu 5/8/08	5/19/08
17	Finishing touches or catch up	14 days?	Fri 5/16/08	d 6/4/08
18	Chirag learn git	6 days?	Wed 4/2/08	d 4/9/08
19	Antonio learn Ltspice	7.5 days?	Tue 4/8/08	4/17/08
20	Chirag request quote #3	2 days?	Wed 4/2/08	u 4/3/08
21	Chirag give quote #3 to Cindy	1 day?	Fri 4/4/08	ri 4/4/08
22	Himanshu setup LTspice and git	3 days?	Wed 4/2/08	ri 4/4/08
23	Himanshu find critical voltages of tinv	3 days	Mon 4/7/08	d 4/9/08



Project: Spring 2008 Schedule
Date: Wed 4/2/08

Task	Milestone	External Tasks	
Split	Summary	External Milestone	
Progress	Project Summary	Deadline	