TERNARY LOGIC IN DIGITAL COMPUTERS

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Introduction

Although the states as well as the number representation of virtually every digital computer are implemented for the most part with binary logic, there are other systems such as the ternary or quinary that could just as well be used. The choice of which logic system to use should be determined primarily on the basis of cost, reliability, and operating speeds of the physical realization. This paper will be concerned with the potential of ternary logic, advantages of this logic, and whether in the future it could be expected to be utilized in digital systems.

Actual Applications of Ternary Logic

Recently, there have been several instances reported where ternary logic and switching circuits have found practical application.

Ternary Arithmetic Application The SET'UN, a Russian stored program computer, incorporates the ternary number system in its arithmetic unit.[1] The mechanization is not wholly ternary since the control logic is binary and information is binary encoded for storage in the bulk and random access memories. Evidently the SET'UN was so designed to take advantage of the relative ease of representing negative and positive numbers and the simplicity of performing round-off when using the ternary representation

$$x = x_{n-1}\, 3^{n-1} + x_{n-2}\, 3^{n-2} + \ldots + x_o,\ x_i = -1,\ 0,\ +1 \qquad (1)$$

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For example, the range [-4, +4] has the representation

x	x_2	x_1
-4	-1	-1
-3	-1	0
-2	-1	1
-1	0	-1
0	0	0
1	0	1
2	1	-1
3	1	0
4	1	1

A negative number, for example -x, has the representation

$$-x = (-x_{n-1})\, 3^{n-1} + (-x_{n-2})\, 3^{n-2} + \ldots + (-x_o) \qquad (2)$$

Thus there is no need to perform an analogous 1's or 2's complement operation as in binary representations.

In rounding off

$$x/3^k = x_{n-1}\, 3^{n-1-k} + x_{n-2}\, 3^{n-2-k} + \ldots + x_k + \ldots + x_o\, 3^{-k}$$

to the nearest integer, only the first n-k significant digits need be used since

$$-\tfrac{1}{2} < x_{k-1}\, 3^{-1} + x_{k-2}\, 3^{-2} + \ldots + x_o\, 3^{-k} < -\tfrac{1}{2}$$

provided of course x_i = -1, 0, and +1. Unlike in the binary case, the k^{th} least significant digit need not be examined to round-off to the nearest integer.

Content Addressable Memories Many of the content addressable memories which have been built or proposed utilize tristable switching in accomplishing a number of operations. For example, the masking of designated stages of the comparison register during interrogation is accomplished by tristable switches and memory drivers. One approach proposed for obtaining efficient retrieval

of ordered lists from a content addressable memory[2] and another for the storage of the three possible responses from each memory register during inequality comparison characterize other areas where tristable circuits could be effectively utilized.

Hazard Free Network Design Ternary switching theory has been proposed as a useful means of designing hazard free binary gate and series parallel contact networks.[3] For example, the Post Algebra compositions min (x, y) and max (x, y) with the one-place function $\bar{x} = 1 - x$ where x and y take on values 0, $\frac{1}{2}$, 1, can be used to design circuits with nominal static states 0 and 1. Since the min and max composition realizations are also the AND and OR gate realizations for binary, it turns out that the Post Algebra can be used to obtain networks which will not produce spurious 0-outputs during input variable transitions between pairs of 1-output conditions, and vice versa.

Other Applications In communications, a three-signal-level transmission technique, duobinary, has been found useful in increasing the channel information capacity with only slight S/N ratio degradation.[4] NASA has actively supported the development of tristable fluid logic devices for hydraulic switching systems.[5] Still another area which is beginning to receive some attention is the use of ternary logic redundancy in binary networks to improve operating reliability.[6]

Applications for Ternary Logic in Digital Systems

Recent advances in the integrated digital circuit and accompanying batch fabrication technology have resulted in substantial reductions in the costs and dimensions of switching networks. Moreover, the reliability and operating speeds of such networks are increasing to the point where the major design problems now arise with interconnecting the circuit modules and allowing for propagation delays between modules.

If ternary logic were to be used in place of binary logic, approximately 37% fewer digits would be required to represent the internal states of a computer. Consequently, for a given machine designed with ternary logic, there would be 37% fewer register and arithmetic stages (for a parallel organization) with a corresponding reduction in the number of control gates. This could be expected to effect a proportionate reduction in the number of curcuit modules, module interconnections and arithmetic carry and other propagation delays. These advantages can only be realized at the expense of somewhat more complex circuit modules, however.

There is some question as to whether the above circumstances alone justify extending the utilization of ternary logic and tristable switching circuits in digital systems. While there appear to be no basic difficulties in developing satisfactory ternary switching devices, and tristable flip-flops and random access core buffers, at present no suitable low cost memory medium has been discovered which would serve as adequate bulk storage as magnetic tape, drum and disc systems do in existing binary machines. Therefore, in addition to special circuit hybrids like those used in content-addressable memories, for example, it appears that ternary logic will be limited to applications not requiring bulk storage such as digital control systems, automatic telephony, and similar special purpose computer systems.

State-of-the-Art in Tristable Circuits

A great deal has been reported in the literature on the mechanization of tristable switching and memory devices; some of the more promising developments will be briefly described below.

A two aperture square-loop ferrite device has been built to exhibit three states in the center leg: saturation up, saturation down, and nonsaturation, by suitable application of MMF to the outer legs. This element could be used as a destructive readout storage element in a coincident select configuration or as a switching device. To obtain useful switching functions it is necessary to operate the core with two and three phase clocked drivers.[7]

Another magnetic element of interest is constructed of glass tubing coated with a thin film of Ni-Fe alloy deposited in a magnetic field. The resulting anisotropy produces a square loop characteristic circumferentially and a linear low coercive characteristic axially. By generating external MMF's both axially and circumferentially, it is possible to achieve either clockwise saturation, counterclockwise saturation, or no saturation in the circumferential direction. This element is well suited for coincident current memory systems.[8]

Still another approach in magnetic elements involves the use of two dissimilar square loop materials either as toroidal cores in a compound configuration or as thin films separated by an insulation layer. By proper selection of the geometry and/or materials it is possible to obtain the tristable hysteresis characteristics shown in Fig. 1. Coincident selection operation requires that in

State 1 a and b are reset: $I_x + I_y < - I_b$

State 2 a is set and b is reset: $\frac{1}{2} I_a < I_x$, $I_y < \frac{1}{2} I_b$ and $I_a < I_x + I_y < I_b$

State 3 a and b are set: $I_x + I_y > I_b$

Constructing a compound core plane should be comparable to the process in the binary case, however, the driving and sensing circuitry and core characteristics will differ and must be held to closer tolerances.

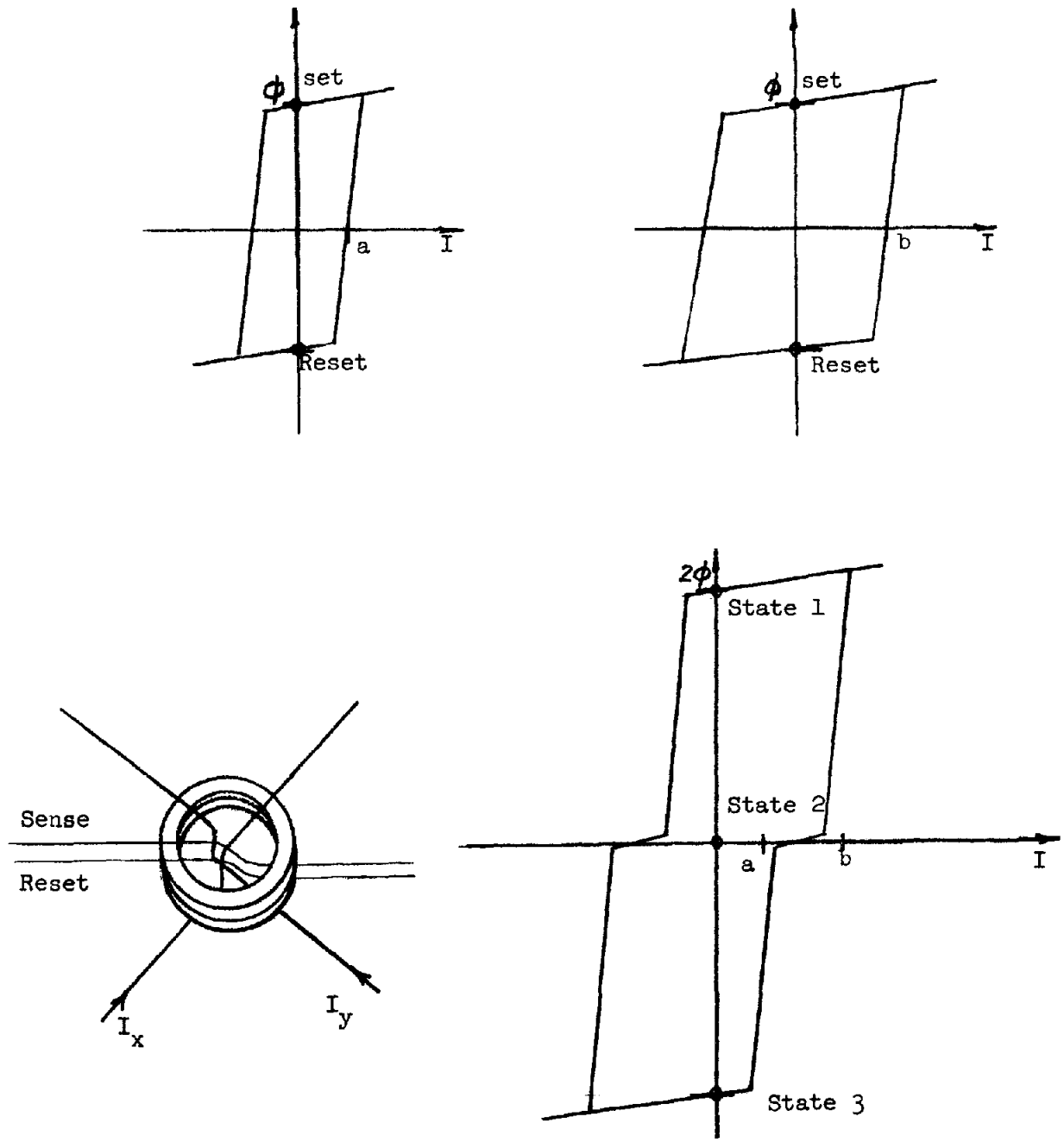


Fig. 1 Compound Square Loop Characteristic

A single tunnel diode circuit has been constructed which exhibits three stable states. It was found that coupling memory stages using a particular two transistor circuit produced a ternary shift-register that shifts in less than 20 nanosec.[9]

Tristable flip-flops which use two transistors where A on B off, B on A off, and A and B off were used to achieve the three stable states have been successfully operated by several people.[10]

Cryogenic storage devices have been built to exhibit three stable states using clockwise, counterclockwise and zero persistent loop currents. Such devices have been constructed on the principle of variable loop segment inductance using three cryotrons per cell[11] and the constant fluxoid effect using two cryotrons per cell.[12] Both approaches appear to be amenable to batch fabrication techniques and quite feasible when reliable and economical cryostats become available.

State-of-the-Art in Logic Design

Various switching circuits which have been reported in the literature are generally based on a set of gating functions held to be well suited for logical design purposes (like AND, OR and NOT functions are in binary logic, for example.) Basically, this means the set of gating functions are functionally complete (can be used to express any of the 3^{3^n} ternary switching functions of n variables) and can be expected to yield economical network realizations. Unfortunately, this field requires much more study before the logical designer can be reasonably assured of having at his disposal near optimal gating functions from both the synthesis and physical mechanization standpoint.

However, two groups of functions warrant consideration: the Post Algebra compositions[13] and the class of compositions which can be expressed as threshold logic functions.[14] Recently, at least two groups have developed logical design techniques for Post Algebra.[8,15] These gating functions are particularly interesting since they have most of the logical and algebraic properties (i.e., associativity, distributivity, commutativity, etc.) exhibited by the AND, OR and NOT binary functions. Moreover, the physical realizations with diode logic, for example, are exactly those for the AND and OR binary functions. The circuit problem of signal level regeneration and inversion, however, is not a simple one since three level rather than two level quantization is required.

Threshold logic has been considered by Hanson,[16] and this author with others.[14,17] Threshold functions are characterized for the two input case as

$$f(x, y) = \begin{cases} 1 & \text{if} \quad w_x x + w_y y \geq t_+ \\ -1 & \text{if} \quad w_x x + w_y y \leq t_- \\ 0 & \text{otherwise} \end{cases}, \quad x, y = -1, 0, +1 \qquad (3)$$

where the parameters w_x, w_y, the weights, and t_+, t_-, the thresholds, are real constants selected for the given $f(x, y)$. This class of functions is of interest because it makes up a large proportion of the ternary gating functions which appear as likely candidates for use in logical design. For example, 15 of the 27 1-place functions and 471 of the 19,683 2-place ternary functions are threshold expressions.[14] Moreover, for reasonable numbers of inputs there are several simple and straightforward mechanizations available such as the parametron circuit with a detuned resonant tank,[18] the non-linear Hall Effect device,[19] and the Kirchoff adder circuit coupled to a "back-to-back" 2-transistor

configuration giving the thresholds for three level quantization. This last circuit is also useful for signal regeneration and inversion required in the Post Algebra diode logic mechanization.

Some Interesting Ternary Logic Networks

Serial Addition In designing digital systems there often is a need for summing and/or counting discrete signals. The typical example is a serial adder in which two numbers x and y are to be summed sequentially. If x and y are ternary encoded as in Eq. (1), then it is well known that the threshold network in Fig. 2 gives the full adder realization.[16] (As shown, each threshold device operating as suggested by Eq. (2) is represented by a circle, the thresholds appear in the form t_+/t_- within the circle adjacent to the output, and the weights appear within the circle adjacent to their respective inputs.)

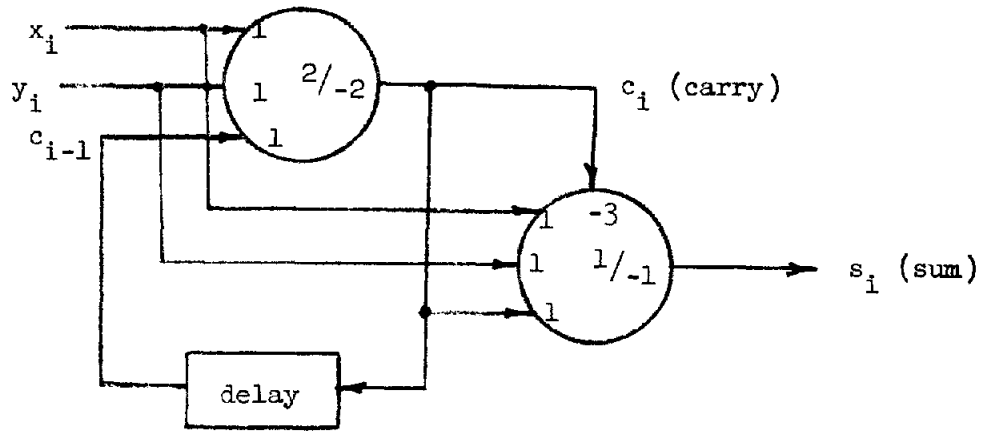


Fig. 2 Serial Adder

Correlation and Averaging A more interesting problem arises in digital control applications where often there is a need to perform such operations as digital correlation

$$\underset{xy}{\Phi}(n) = \frac{1}{2NT} \sum_{k=-N}^{N} x_k \, y_{k+n} \quad , \quad T = \text{sampling period}$$

or ensemble averaging

$$\langle z\,(n)\rangle \;=\; \frac{1}{N}\sum_{k=1}^{N} z^{k}\,(n)$$

If a combinational mechanization is desired for speed or some other considerations, then there can be definite advantages to using ternary logic. The most significant aspect is that both negative and positive signals can be summed without special network provisions. For example, consider the ternary threshold network for summing the function $\sum_{k-1}^{M} x_k$ when x_k = -1, 0 or +1. The Fig. 3 network provides the sum in the Eq. (1) weighted ternary code. It has been shown that

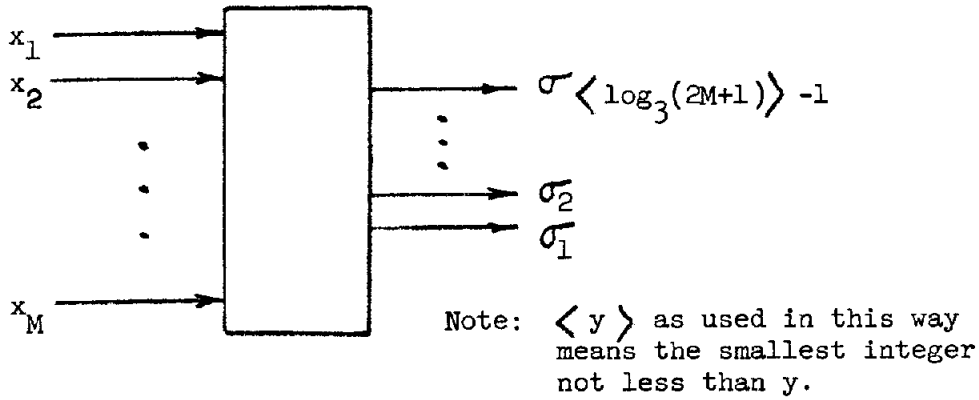


Fig. 3 General Counting Network

this network can be realized with $\langle \log_3 (2M + 1)\rangle$ -1 threshold devices as shown in Fig. 4 which is the minimal number for this network.[17] There are techniques for decomposing this network into a network of modules where each module is a network of threshold devices satisfying some practical physical constraints.[20]

The approach taken in Fig 4 can be adapted to the more general situation where each

$$x_k = 3^{n-1}\, x_k^{n-1} + \ldots + x_k^{o} \quad , \; x_k^{i} = -1,\ 0,\ +1$$

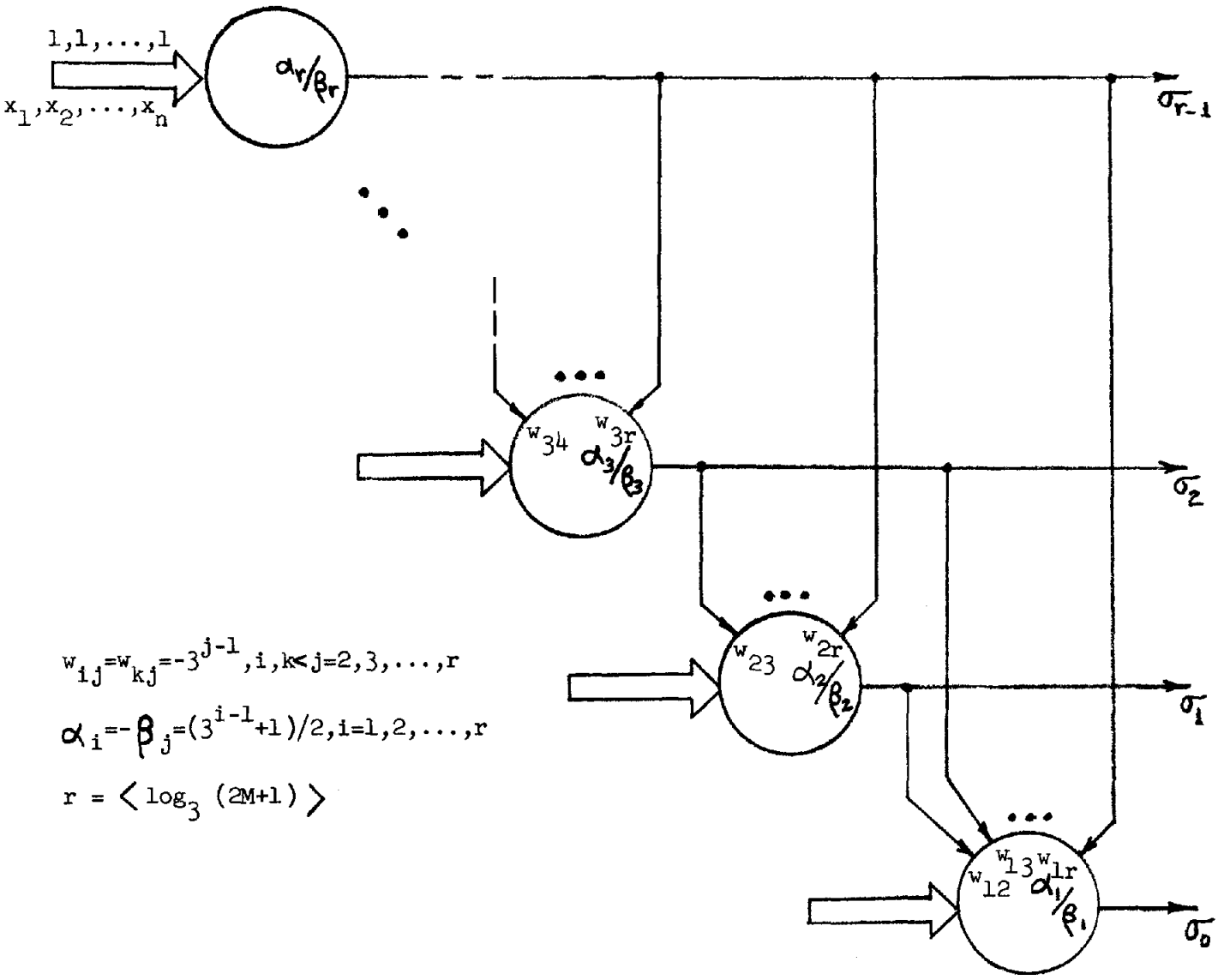


Fig. 4 Feedforward Threshold Network

by summing all x_k^i , k = 1, 2, ..., M with a Fig. 4 network whose outputs σ_j^i in the weighted ternary representation, Eq. (1), are weighted by 3^{i+j} . There will be n such networks, the outputs of which can be summed in the same manner as were the x_k^i . This synthesis process is repeated in much the same way suggested by Fig. 4 to obtain the final realization.

Redundancy Logic Earlier, it was mentioned that ternary logic could be used to achieve more reliable binary networks. It has been suggested that ternary majority gates could be used in this way to construct a reliable binary flip-flop. The well known circuit shown in Fig. 5 using triple redundancy and

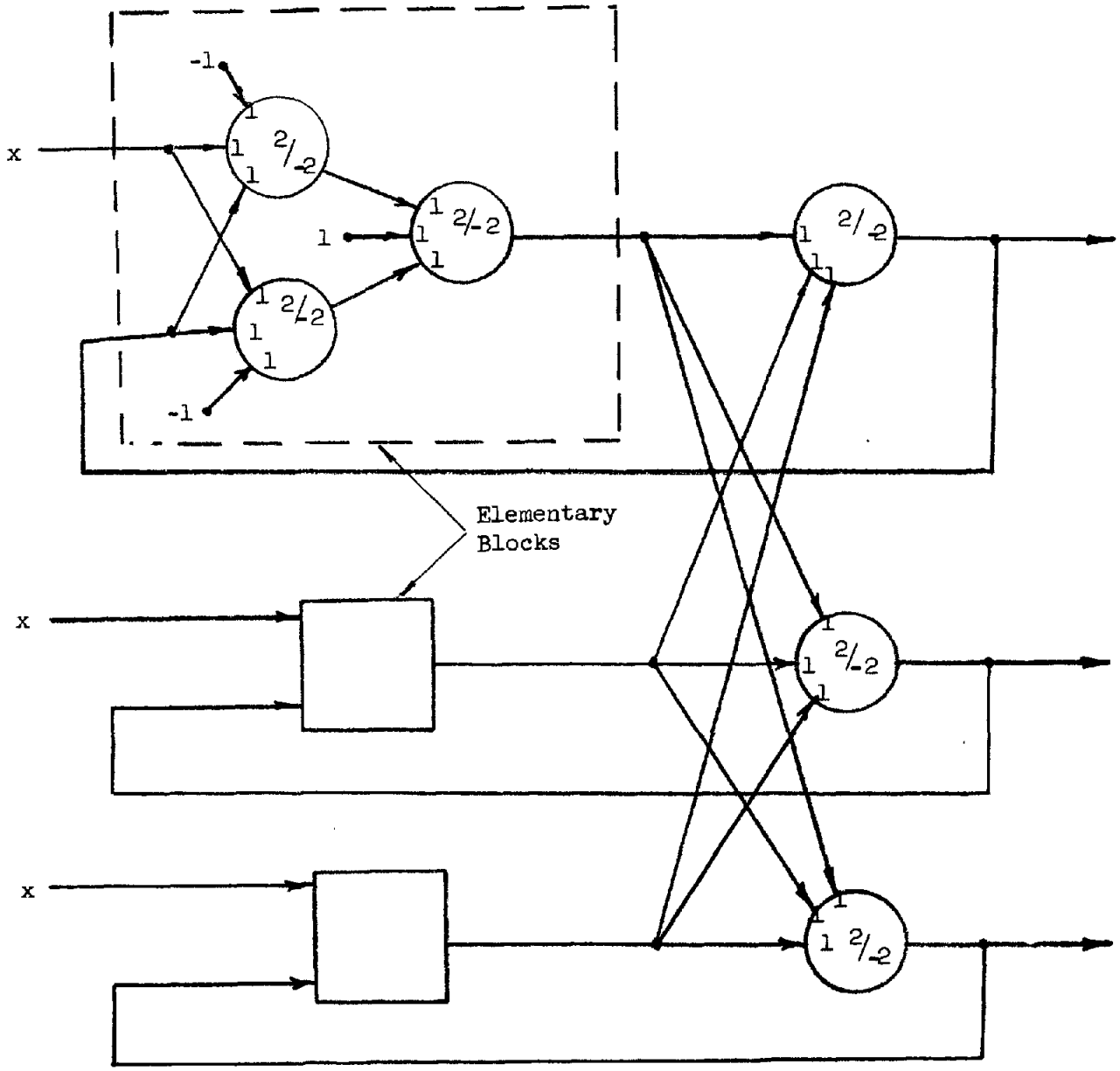


Fig. 5 Triple Redundant "Voting" Logic Flip-Flop

"voting" logic will, for the binary gate implementation, contrive to operate correctly in the event of failure of any one element or any one connection. Using ternary gates correct operation is realized in three situations: (1) when all these elementary levels operate correctly, (2) when one block gives nonzero incorrect responses, and the two others operate correctly, and (3) when two blocks give zero responses and the third operates correctly.[6]

Conclusions

In this paper the current state-of-development in ternary logic and switching circuitry have been summarized. In addition, some of the significant applications, potential as well as actual, have been described. At the present time the following general conclusions can be stated:

(1) With the existing lack of good ternary bulk storage, and fast simple binary-ternary encoders, the application of ternary logic will be limited to digital systems which have no such memory requirements.

(2) The advantages to be gained with ternary logic in requiring fewer digits (hence fewer registers, arithmetic, and control stages), and possessing simpler means of representing positive and negative numbers and rounding-off must more than compensate for the increased gating and memory circuit complexity before it will take the place of binary logic.

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