IMPLEMENTATION OF 3-VALUED LOGIC WITH C.O.S. M.O.S. INTEGRATED CIRCUITS

Indexing terms: Integrated circuits, Ternary logic

Two ternary gates realising basic ternary operators (ternary NOR, NAND and invertors) are designed with c.o.s.m.o.s. integrated circuits. Any one of these gates may be used to implement several 3-valued algebras.

• The availability of ternary memory elements as well as a complete line of ternary logic circuits at a reasonable cost is necessary for a wide application of ternary systems.[1, 2] This problem may be solved by an application of the complementary-symmetry metal oxide semiconductor (c.o.s.m.o.s.).[3-5]

In this letter. a new c.o.s.m.o.s. ternary gate is presented, permitting implementation of several ternary functions. The three voltage levels of ternary logic circuits will be presented here by 0, 1 and 2: 0 for the low (−4 V), 1 the intermediate (zero potential) and 2 the high level (+4 V).

Two different circuits have been constructed to realise the ternary a.o.i. (AND–OR–invert) gate. Fig. 1 shows a schematic of a ternary a.o.i. gate constructed with three *n* channel and three *p* channel enhancement-type m.o.s. transistors. The circuit has three outputs to perform five functions: the simple ternary invertor (s.t.i.), the positive ternary invertor (p.t.i.), the negative ternary invertor (n.t.i.), the ternary NOR (TNOR) and the ternary NAND (TNAND). These functions were defined[5] by

$$\text{s.t.i.} \equiv \overline{x^1} = 2 - x$$

$$\text{p.t.i., n.t.i.} \equiv \overline{x^i} = \begin{cases} i & \text{if } x \neq i \\ 2-i & \text{if } x = i \end{cases}$$

where i can be 0 or 2. The minus sign in the previous equations represents arithmetic subtraction.

$$\text{TNOR} \equiv \overline{(x+y)^1} = \overline{\max}\,(x, y)$$

$$\text{TNAND} \equiv \overline{(x \cdot y)^1} = \overline{\min}\,(x, y)$$

Truth tables for the above ternary basic operators are given in Table 1. In Fig. 1*a*, two *p* channel devices in series are in parallel with a *p* channel device, and two parallel *n* channel devices are in series with an *n* channel device. The operation of this circuit can be briefly described as follows:

When the input X (or Y) is 2 (high level), transistor n_1 (or n_2) will be on, permitting the use of p_3 and n_3 as a s.t.i., p.t.i. or n.t.i. circuit, depending on which output is taken:

p.t.i.: $A = \overline{Z^2}$

s.t.i.: $B = \overline{Z^1}$

n.t.i.: $C = \overline{Z^0}$

Table 1 TRUTH TABLES OF FIVE OPERATORS REALISED BY CIRCUIT OF FIG. 1

a

x	$\overline{x^2}$	$\overline{x^1}$	$\overline{x^0}$
2	0	0	0
1	2	1	0
0	2	2	2

b

x	2	2	2	1	1	1	0	0	0
y	2	1	0	2	1	0	2	1	0
$\overline{(x+y)^1}$	0	0	0	0	1	1	0	1	2
$\overline{(x \cdot y)^1}$	0	1	2	1	1	2	2	2	2

The circuit will be used as a TNAND gate when the input X is 0. In this case, p_1 will be on and channels p_2, p_3, n_2 and n_3 will form the TNAND gate, giving

$$B = \overline{(Y \cdot Z)^1}$$

Channels p_1, p_3, n_1 and n_3 will form also a TNAND gate if the input Y is 0, because the p_2 channel will be on. In this case,

$$B = \overline{(X \cdot Z)^1}$$

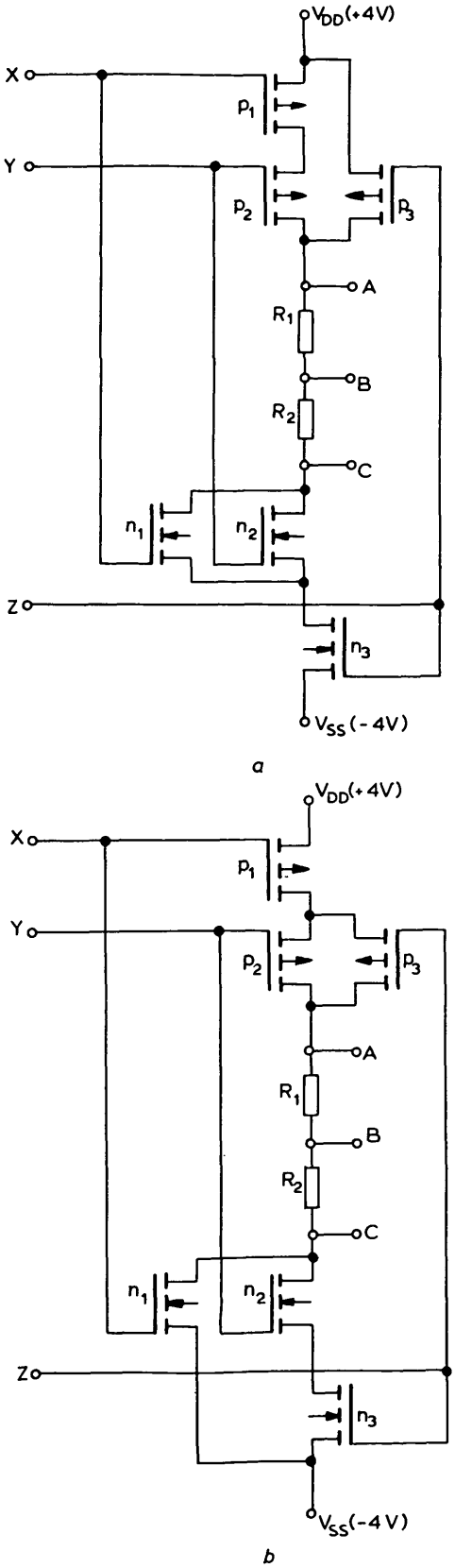


Fig. 1 *Ternary a.o.i. circuit*
A ≡ output of p.t.i.
B ≡ output of TNAND, TNOR and s.t.i.
C ≡ output of n.t.i.
All *p* unit substrates are connected to V_{DD} and all *n* unit substrates are connected to V_{SS}
$R_1 = R_2 = 12\ \text{k}\Omega$

A TNOR gate could be also realised if input Z is 2. Channels p_1, p_2, n_1 and n_2 will form this gate, because p_3 is off and the output will be

$$B = \overline{(X+Y)}^1$$

Therefore it can be concluded that the output B realises the function

$$B = \overline{(X+Y\cdot Z)}^1$$

The same function is realised by the application of the circuit of Fig. 1*b*. It has to be noted that the operation of this circuit will be slightly different from that of Fig. 1*a*. The circuit of Fig. 1*b* will be used as any invertor if the input Y or Z is 0, as a TNAND gate if X is 0 and as a TNOR gate if Y or Z is 2.

One of the two circuits presented here will be sufficient for the implementation of algebras due to Rosser and Turquette, Lee and Chen, Yoeli and Rosenfeld and Halpern and Yoeli.[1-3] By the addition of the two basic ternary operators, the forward diode (f.d.) and the reverse diode (r.d.), one can easily implement algebras due to Post, Vacca, Mine *et al.* and Mouftah and Jordan.[3, 5] The two operators f.d. and r.d. were previously defined by

$$x^{K_i} = \begin{cases} 1 & \text{if } x \neq i \\ i & \text{if } x = i \end{cases}$$

where i can be 2 or 0, K_2 represents the f.d. operator and K_0 the r.d. operator.

Conclusion: C.O.S.M.O.S. integrated circuits may be applied to construct a ternary gate able to implement several 3-valued switching algebras. A set of five ternary operators may be realised by the same circuit, which represents an advantage from the technological point of view. This may facilitate the use of ternary digital machines.

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PARAMETRIC AMPLIFICATION OF ACOUSTIC SURFACE WAVES ON CdS

Indexing terms: Acoustic-surface-wave devices, Parametric amplifiers

We report some experimental results on the parametric interaction of codirected s.a.w. in photoconducting CdS. This interaction takes place through the 2nd-order electric field associated with the bunching of carriers. Below threshold conditions, we directly observed both parametric attenuation and amplification with a 30 dB dynamic range. At the highest electric level of the pump available on our apparatus, 16 dBm, the parametric gain is about 10 dB. Beyond the threshold conditions, we observed only a parametric attenuation.

Introduction: We report some results on parametric effects of acoustoelectric origin that take place during the propagation of codirected surface waves on photoconducting CdS.

Experiments: On a p.q.o. face of the crystal are two sets of interdigital transducers acting as transmitters and receivers at frequencies of 30, 40 and 70 MHz. An active part of a segmented amplifier type, with 8 cells, analogous to the one described in Reference 3, is diffused between the two systems of transducers. A mobile screen allows one to vary the number of cells illuminated, i.e. the length of interaction. Two waves are launched on one extremity of the sample. The first is at a high level, and is denoted by U_3, and constitutes the pump at a frequency $f_3 = 40$ MHz. Its duration is 1·5 μs. The second is at a lower level at a frequency $f_2 = 70$ MHz, and is the signal; its duration is 4 μs. Its amplitude, denoted by U_2 in the absence of the pump and $U_2^{(2)}$ during its presence, is measured on the other side of the structure.

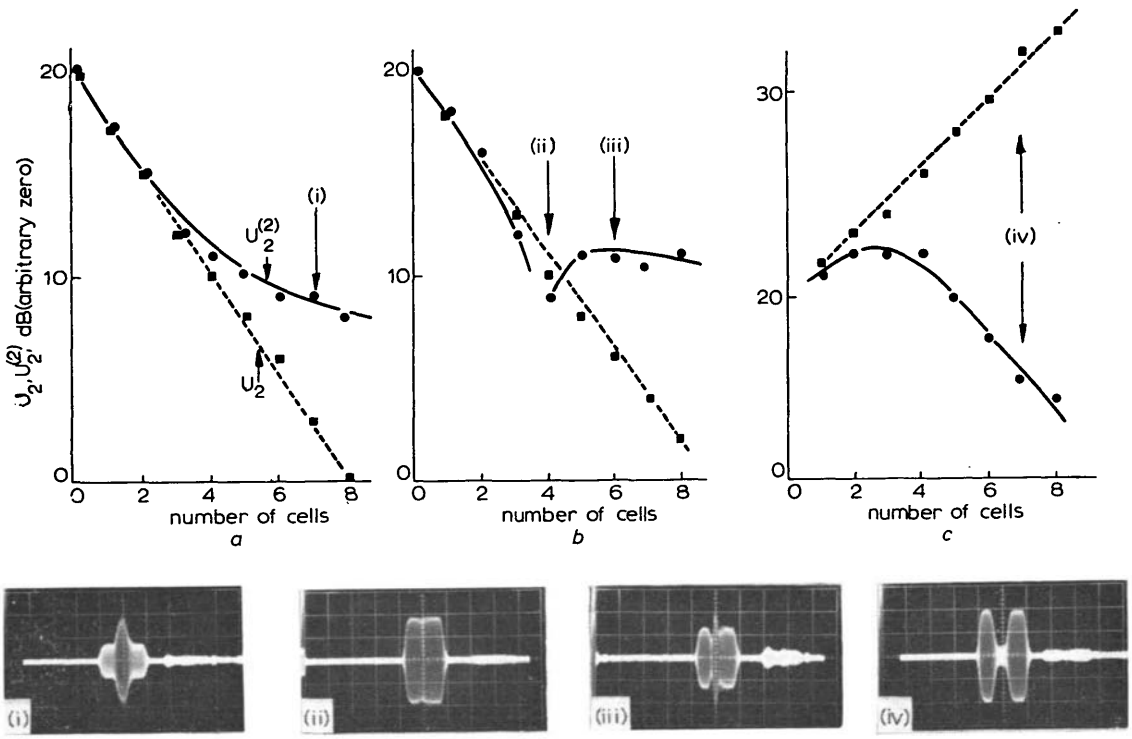


Fig. 1 *Experimental variation of output signal against interaction length*
Accelerating voltage:
(*a*) $V_0 = 60$ V
(*b*) $V_0 = 80$ V
(*c*) $V_0 = 145$ V.
Interaction length = 0·5 mm (each cell)