The High Speed Ternary Logic Gates Based on the Multiple β Transistors

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[Abstract] This paper develops a kind of multiple β transistor based on the multiple-emitter transistor whose emitter has different current gain β. And then presents the design of the linear AND/OR gates and multi-valued literal circuits. These two kind of circuits have not only simple structure but also very high operating speed, so that they can be utilized to the design of the high speed multi-valued logic circuits.

I.Introduction

Consider ternary logic as an example. The following three basic operations are composed to a complete set:

AND operation: $x \cdot y = min(x,y)$ (1)

OR operation: $x+y = max(x,y)$ (2)

Literal operation:

$$^{i}x^{j} \equiv \begin{cases} x, & \text{where } x=i \\ 0, & \text{where } x<>i \end{cases} \quad (3)$$

where x,y,i∈{0,1,2}. Obviously, if a function is shown by these three basic operations, the corresponding basic gates of the ternary logic circuits are AND gate, OR gate, and Literal circuit. Therefore, the circuit design of these basic gates becomes the base of multiple-valued logic circuit design.

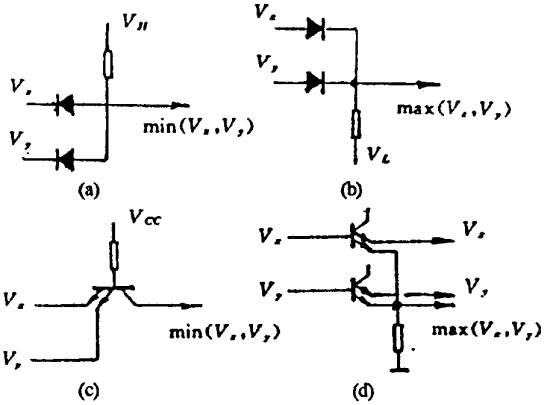


Fig.1 AND/OR operation by PN Junction
(a)diode AND gate (b)diode OR gate
(c)AND operation by input emitters of a transistor
(d)OR operation by output emitters of a transistor

From the definitions of equation (1)(2), it is shown that the AND/OR operations are inherently comparation and selection between signals. If the voltages are as signals, based on the PN Junction forward characteristics, it is easy to realize min/max operation between signals, that is AND/OR operation. Fig.1(a)(b) show respectively AND gate and OR gate with diodes, which are adaptable for both 2-valued and multi-valued signals. This fact hints that the multi-valued gate circuits with simple structure might be realized by PN Junctions of bipolar junction transistors.

For transistors to realize AND/OR operation, we can manufacture transistors in the multiple-emitter structure[1], which can be easily realized by adding emitter regions on P base in technology. While considering the multi-emitters as the multiple diodes with P region contact, AND operation of the input signals of emitters is realized, as shown in Fig.1(c), whose structure has been applied to realize AND operation of the input signals of TTL circuits. And similarly to the structure of Fig.1(b), while applying the emitters as outputs, OR operation between multiple outputs is obtained, as shown in Fig.1(d). In fact, this wired-OR function is often applied in 2-valued ECL circuit design. It is noted that in Fig.1(d), multiple-emitter structure is applied, so that both the wired-OR operation of output signals can be realized and the original output signals can be remained simultaneously.

From the above discussion, it is shown that after the transistor structure is developed from single-emitter to multiple-emitter, its logic function is highly enhanced and the design flexibility is improved. Based on the emitter junction forward characteristics, AND (while emitters used as inputs) and OR (while emitters used as outputs) operations are simply realized. However, one transistor can not simultaneously applied as both AND and OR operations.

Furthermore, it is supposed that if the multi-emitters of a transistor be further developed from the conventional single current gain to multiple current gains then with the rich of the transistor physical structure, its logic function could be further enhanced with high design flexibility. Especially for the multi-

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valued logic circuits that can process much information, we have successful experience of applying multi-threshold MOS transistors[2-4], so that introducing this kind of multiple β bipolar transistors should meet the needs of the multi-valued logic circuit design. In this paper, the design and the characteristics of the basic ternary gate circuits with the multiple β transistors are focused.

II.The Linear AND/OR Gates Based on the Multiple β Transistors

We consider the multiple β transistors have two emitters with two different current gains[5], shown as Fig.2(a), where the β_i of the side-base emitter is very small about 0.2; and the β_o of the side-collector emitter is normal, e.g. β_o=10~50, and in technology, firstly on n-type substrate, once thick boron deep diffusion and once thin boron shallow diffusion, and secondly once phosphorus diffusion to form small β_i and normal β_o emitter regions respectively on thick and thin boron regions. Fig.2(b) is the section view of the multiple β transistor, in which the resistance R_b for base junction current is formed directly by extending boron layer and n-type base is contacted directly to the power supply without isolation islands.

In the multiple β transistor shown as Fig.2(a), the emitters with small β_i are applied as inputs, and those with normal β_o as outputs. In this way, its input method is similar to TTL circuits that can make AND operation for input signals, while its outputs method is similar to ECL circuits that can make wired OR operation by interconnecting with other outputs, shown as Fig.2(c). So the multiple β transistor can combine AND/OR function by itself. The linear AND/OR gate was realized based on the multiple β transistor by Wang [5]. Comparing to the diode AND/OR gates, there are many advantages. Firstly there does not exist basically voltage deviaton between output and inputs since the two emitter junction voltages of the multiple β transistor are offset each other, secondly the multiple β transistor can amplify its inputs current because of the considerable difference of β_i and β_o, and moreover there is linear relation between output and input because the two emitters are conductive while the multiple β transistor is operated normally in linear active region, and the circuits in Fig.2(c) are therefore referred to "Linear AND/OR gate".

Based on the circuits in Fig.2(a), the paper[6] further presented a kind of improved active feed Linear AND/OR gate, shown as Fig.3(a). What is called "active feed" means that the base current of the multiple β transistor is supplied by a constant current source which is formed by a lateral PNP transistor.

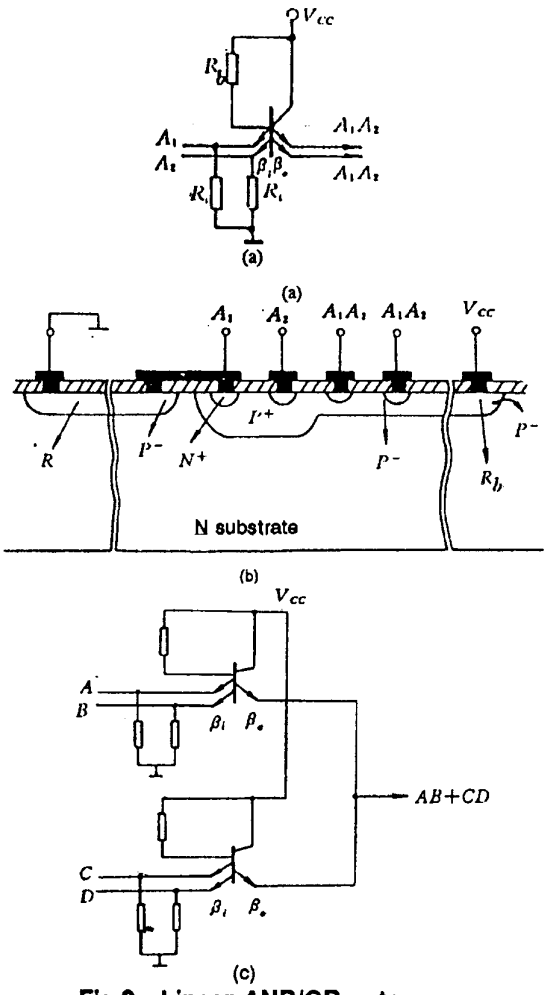


Fig.2 Linear AND/OR gates
(a)multiple β transistor (b)section view
(c)linear AND/OR gates

These two kinds of linear AND/OR gates based on the multiple β transistor have not only simple structure and power logic functions but also high speed characteristic, the reasons are as follows:

(1)their collector is fully grounded for alternating current, so there does not exist the problem "isolation island's capacity affects speed" as common integrated logic circuits do.

(2)while changing states, the charging voltage of collector capacity is only the logic swing not the approximately doubled.

(3)they are emitter follower like nonsaturation circuits.

(4)since the current amplification and the small voltage deviation, they can be applied in multiple cascades without necessity of restoration each stage, so that the delay by level restoration cell may be

decreased (note that the main delay of gate circuits is resulted by level restoration part).

As an example, we have made SPICE emulation for 5-stage circuit with the active feed linear AND/OR gates with following conditions: given V_{cc}=5v, base current source I_o=1.6mA, β_i=0.2, β_o=10, the inputs of the circuit are ternary signals (1.8v, 2.6v, 3.4v), considering the all possible signal transitions. The transient analysis curve of the circuit is shown in Fig.3(b), where, the average propagation delay of the 5-stage circuit is tested as 1.26ns and the average voltage deviation as 0.16, that is to say, for a single linear AND/OR gate, the average propagation delay is only 0.25ns, and the average voltage deviation is only 0.03v. It is proved that the two characteristics of super high speed operating and multistage applications of linear AND/OR gates. In fact, to investigate the application ability of the linear AND/OR gates, the experiments was made by washing emitter technique, under 6 μm technology, the typical average propagation delay per gate is 0.3ns and the product of delay and power consumption is 2.1pJ[6], whose speed is much higher than IIL. Furthermore a 12bit × 12bit high speed binary array multiplier with 9-stage structure based on multiple β transistors was developed in the Institute of Semiconductors of Academia Sinica in 1990. Under 6 μm technology, the whole propagation delay of the developed circuit was tested as 10ns[7], which proved once again the above two characteristics.

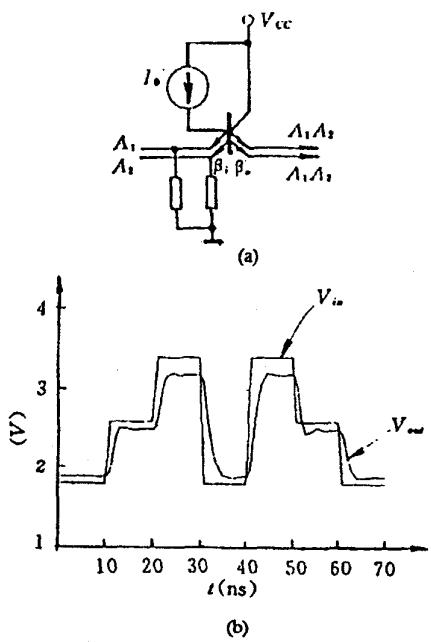


Fig.3 Active Feed Linear AND/OR Gate
(a)circuit structure
(b)transient analysis curve of 5-stage circuits

Although the multiplier design example is binary circuit, from the definitions of Equ.(1) and (2), we can see that the multiple β transistor can be applied to multi-valued signals too. The circuits of Fig.2(a) and Fig.3(a) can also be done as the multi-valued linear AND/OR gates to realize the multi-valued AND/OR operations.

III.Ternary literal circuits based on the multiple β transistor

The linear AND/OR gate discussed above is of super high speed operating characteristic, but has not the level restoration function. Therefore the literal circuit to realize the another basic operation---literal operation must have the restoration function, so that the practical ternary logic circuits can be composed with the linear AND/OR gate. Since the considerable difference between the two βs of the multiple β transistor, the ternary literal circuit can be designed whose structure is similar to Fig.3(a), shown as Fig.4(a), where the emitter with β_o is contacted to reference voltage V_r and its collector is contacted to the source V_{cc} by a resistance R. The operating principle of this circuit is as follows: while $V_x<V_r$, I_o is injecting the emitter with β_i, the collector current will be $\beta_i I_o$, since β_i=0.2, the voltage drop across the resistance R is very small; while $V_x>V_r$, I_o is injecting to the emitter with β_o, the collector current will be $\beta_o I_o$, at this time, the voltage drop across R will be bigger, but because of the voltage clamp by the diodes in the two series, the output of the collector will be limited to V_{cc}-1.6v. In this way, in Fig.4(a), through the voltage level shifting by the emitter follower and the other diode circuit, the output of the collector made of the multiple β transistor will be the binary signal (1.8, 3.4) corresponding to the logic value (0, 2). Obviously, while given V_r=2.2v and 3.0v in Fig.4(a), the output of the circuit will be respectively $^0x^0$ and $\overline{^2x^2}$.

It should be pointed that, if the multiple β transistor in Fig.4(a) is decomposed two transistors whose collectors and bases are connected in paralleled, it will present the structure of differential transistor pair similar to ECL and will be also a kind of nonsaturation switch so that it may be of very high operating speed like ECL. Let V_r=2.2v as an example, Fig.4(a) is the literal circuit to generate $^0x^0$, and Fig.4(b) is the emulated transient analysis curve under the same emulating parameters as before. From Fig.4(b), its average propagation delay is tested as 1.12ns which proves this ternary literal circuit is of high operating speed.

As mentioned above, while V_r=3.0v in Fig.4(a), the literal circuit $\overline{^2x^2}$ will be obtained. And

any other literal circuits will be generated by ${}^{0}x^{0}$ and $\overline{{}^{2}x^{2}}$, therefore with this ternary literal circuit developed in this section and the linear AND/OR gate in section II, various high speed ternary logic circuits based on the multiple β transistor can be designed.

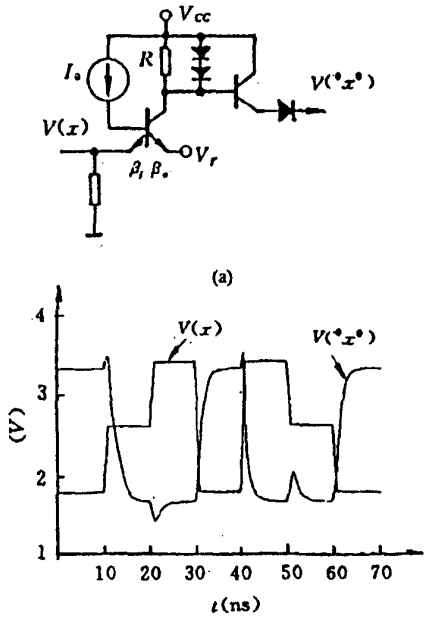


Fig.4 ternary literal circuit.

(a)circuit structure
(b)transient analysis curve of the literal circuit (generating ${}^{0}x^{0}$)

IV.Conclusion

In MOS circuits, the single threshold MOS transistor was developed to the multiple threshold one by adopting the multi-layer ion implantation technology. This measure enriching MOS transistor's physical structure can make a MOS transistor not only store [2,3] but also detect and process the multi-valued information. In this paper, we have presented that in bipolar circuits, the multi-emitter transistor with single β is developed to the multi-emitter one with different β by applying the multi-layer boron diffusion technology. This measure enriching bipolar transistor's physical structure can also enhance the logic functions and design flexibility of the transistors too. The discussion in this paper shows :

(1)a multiple β transistor can combine AND/OR function so that it can be composed as the linear AND/OR gate with very simple structure;

(2)applying the considerable difference of the two βs, the differential nonsaturation switch can be designed easily by only one multiple β transistor, which can complete the multi-valued AND, OR, and Literal basic operations accompanying with the linear AND/OR gate;

(3)since the level restoration function, the Literal circuits can remedy the defect that there is no level restoration function with the linear AND/OR gate.

From the analysis of Introduction, it should be noted that in the linear AND/OR gate and the Literal circuits based on the multiple β transistor, the transistors are all operated in active region without saturation, which can principally ensure these two basic circuits to operate at very high speed. Besides, inputs and outputs in these two circuits are all connected with emitters. This operating method can easily realize AND/OR operation so that the simple circuit design can be obtained. All these characteristics of the logic circuits on the multiple β transistor are worth to be noted.

Acknowledgement:

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