STATIC-HAZARD-FREE T-GATE FOR TERNARY MEMORY ELEMENT AND ITS APPLICATION TO TERNARY COUNTERS

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ABSTRACT

The ternary T-gate can be used as a basic building block to construct both combinational and sequential circuits. For constructing ternary memory elements, however, the T-gate is required to be static hazard-free. A theoretical study is done on the necessary conditions for practical realization of the static-hazard-free T-gate. On the basis of the result obtained, the T-gate for memory elements can be realized. The T-gate is experimentally verified to be static hazard-free. The static-hazard-free T-gate obtained here can be used as building blocks to construct memory elements. We can easily construct various memory elements such as D flip-flap-flop (FFF), D master slave FFF, B master slave FFF, and counting FFF. They are operated satisfactorily. Using these memory elements, three different ternary counters are designed and realized. These ternary counters are superior to the binary ones in that the up-down counting can easily be carried out by one input signal.

I. INTRODUCTION

The ternary T-gate which constructs a complete system [1] can be used as a basic building block to construct both the combinational and sequential circuits [2]. The T-gate will be easily implemented with the development of integrated circuit technology which makes it possible to produce a complex module in one chip. So far, the T-gate has been implemented by various electronic circuits [3-6]. For the purpose of constructing the memory elements, however, the properties which are required of the T-gate have not yet been studied in detail. Moreover, it has not been shown that various types of ternary memory elements and ternary counters can be realized by using T-gates as building blocks.

The T-gate for use in memory elements must be static hazard-free for the change of a control signal. In this paper, first a theoretical study is done on the necessary conditions for practical realization of the static hazard-free T-gate. As a result, a block diagram representing a design method of the T-gate which is static hazard-free is presented. On the basis of the result obtained, the current mode circuit of T-gate is designed and implemented as an example. This circuit is experimentally assured to be static hazard-free for the change of a control signal. The current mode circuit is very suitable for the integrated one, because it consists of only one npn type of transistor and operating speed is principally very fast.

Using the static-hazard free T-gates obtained here as building blocks, we can easily construct the ternary memory elements such as D FFF, D master slave FFF, B master slave FFF, and counting FFF. Their operating properties are studied theoretically and experimentally.

The practical ternary sequential circuit can systematically be realized on the basis of memory elements. As examples of sequential circuits, ternary counters are designed and realized by using these memory elements. In counting the ternary sequence, we assume that the counting pulse is the return-to-zero (RZ) one. Moreover, a positive pulse "1" is counted to the up direction while a negative pulse "-1" is counted to the down direction. Three different counters are presented which are characterized by advantages of the ternary logic system. Their properties and advantages are discussed in view of constructing a ternary digital system.

II. CIRCUIT IMPLEMENTATION OF T-GATE FOR MEMORY ELEMENTS

The ternary T-gate is defined as [1-2]

$$T(p, q, r ; s) = p.J_1(s) + q.J_0(s) + r.J_{-1}(s) \quad (1)$$

where the variables p, q, r and $s \in L = \{1, 0, -1\}$, and where the product $\cdot$, the sum $+$, and J operators are defined as follows:

$$x.y = \min(x, y), \qquad x + y = \max(x, y),$$

$$J_k(s) = \begin{cases} 1 & \text{if } s = k \\ -1 & \text{if } s \neq k \end{cases}.$$

Theorem 1 $$T(p, q, r ; s) = (p + h_1(s)).q.(r + h_{-1}(s)) + p.J_1(s) + r.J_{-1}(s) \quad (2)$$

where h operators are defined as

$$h_k(s) = \begin{cases} -1 & \text{if } s = k \\ 1 & \text{if } s \neq k \end{cases}.$$

proof: h operators are expressed as $h_1(s) = J_0(s) + J_{-1}(s)$ and $h_{-1}(s) = J_1(s) + J_0(s)$ [7]. The given equation is expanded as follows:

$$\begin{aligned} F &= (p + h_1(s)).q.(r + h_{-1}(s)) + p.J_1(s) + r.J_{-1}(s) \\ &= (p + J_0(s) + J_{-1}(s)).q.(r + J_1(s) + J_0(s)) \\ &\quad + p.J_1(s) + r.J_{-1}(s) \\ &= q.(p.r + p.J_1(s) + p.J_0(s) + r.J_0(s) + \\ &\quad J_1(s).J_0(s) + J_0(s).J_0(s) + r.J_{-1}(s) + \\ &\quad J_1(s).J_{-1}(s) + J_0(s).J_{-1}(s)) + p.J_1(s) + \\ &\quad r.J_{-1}(s) \end{aligned}$$

Using the following relationships [7]

$$J_k(s).J_{k'}(s) = \begin{cases} J_k(s) & k = k' \\ -1 & k \neq k' \end{cases}, \quad x + x.y = x,$$

the equation becomes

$$F = p.q.r + p.J_1(s) + q.J_0(s) + r.J_{-1}(s).$$

Since $J_1(s) + J_0(s) + J_{-1}(s) = 1$,

$$\begin{aligned} F &= p.q.r.(J_1(s) + J_0(s) + J_{-1}(s)) + p.J_1(s) + q.J_0(s) + r.J_{-1}(s) \\ &= p.(q.r + 1).J_1(s) + q.(p.r + 1).J_0(s) + r.(p.q + 1).J_{-1}(s) \\ &= p.J_1(s) + q.J_0(s) + r.J_{-1}(s). \end{aligned}$$

Therefore, $T(p, q, r ; s) = (p + h_1(s)).q.(r + h_{-1}(s)) + p.J_1(s) + r.J_{-1}(s)$. Q.E.D.

The block diagram corresponding to Eq. (2) is shown in Fig. 1.

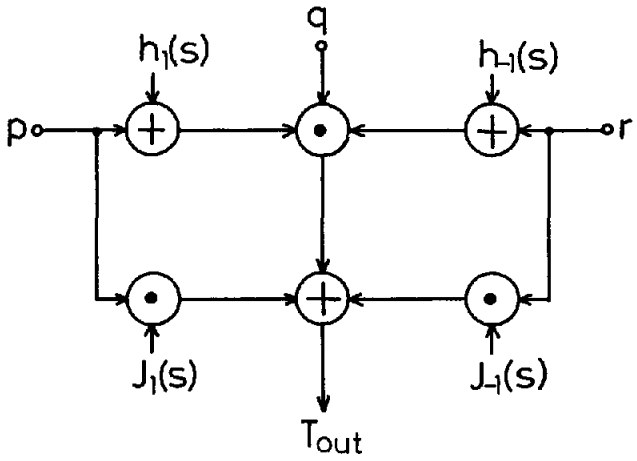


Fig. 1

Theorem 2 When p equals q, and the control signal s is changed from "1" to "0", then the output of the T-gate in Eq. (2) is static hazard-free. Similarly, when r equals q, and s is changed from "-1" to "0", then the output of the T-gate in Eq. (2) is static hazard-free.

proof: In Eq. (2), we consider the case where p equals q and s is changed from "1" to "0". As the $J_{-1}(s)$ is always "-1" and $h_{-1}(s)$ is always "1" even in the transient state of s, $T_{out} = (p + h_1(s)).q.(r + 1) + p.J_1(s) + r.(-1) = (p + h_1(s)).q + p.J_1(s)$. T_{out} becomes as

$$\begin{aligned} T_{out} &= (p + h_1(s)).p + p.J_1(s) \\ &= p.(p + h_1(s) + J_1(s)). \end{aligned} \quad (3)$$

This shows that T_{out} is always p (= q) regardless of the transient state of the control signal s. Similarly, in the case where r equals q and s is changed from "-1" to "0", T_{out} is always r (= q) regardless of the transient state of the control signal s. In other words, under the static conditions, the T-gate as shown in Fig. 1 is a static-hazard-free circuit. Q.E.D.

However, the transient from s = -1 to s = 1 or vice versa is not static hazard-free because s has just a little interval when s goes across "0". Generally, this matter is peculiar to ternary logic unlike the binary one.

2. Current Mode Circuit for Static-Hazard-Free T-gate

In a current mode circuit, the saturation of the transistors is prevented to avoid delay caused by the storage effect. The major advantage of this group of digital circuit [also called emitter coupled logic (ECL)] is therefore its short propagation delay.

Fig. 2 shows the current mode circuit of the T-gate realized on the basis of the block diagram of Fig. 1. In constructing the ternary ECL circuit, we must turn our attention to the level shifting. Let the truth values "1", "0" and "-1" correspond to the voltage $2V_d$, 0, $-2V_d$ respectively. The voltage V_d is denoted as the forward voltage drop of the base emitter diode of a transistor. The circuit is designed so that the operating point of the diodes is set at $V_d = 0.7$ V. The threshold voltage between "1" and "0" is set at V_d and the threshold voltage between "0" and "-1" is set at $-V_d$. These voltages V_d and $-V_d$ are generated at the points G and H in Fig. 2 respectively.

When the positive pulse "1" is applied to the control terminal s, the voltage of the points A and B, V_A and V_B will be $2V_d$ and $6V_d$ respectively. On the arrival of the zero pulse "0" or the negative pulse "-1" at s, V_A and V_B become $6V_d$ and $2V_d$ respectively. Consequently, it can be seen that voltages V_C and V_D are corresponding to $h_1(s)$ and $J_1(s)$ respectively. Similarly, we can say that voltages V_E and V_F are corresponding to $J_{-1}(s)$ and $h_{-1}(s)$. Using emitter follower OR circuits, the voltages V_I and V_K become $(p + h_1(s))$ and $(r + h_{-1}(s))$ respectively. Also, by using multi-emitter AND circuits, the voltages V_J and V_L become $p.J_1(s)$ and $r.J_{-1}(s)$. Thus, it is seen that the voltage V_M equals $(p + h_1(s)).q.(r + h_{-1}(s))$. Now assume that the base voltage of Tr_{19}, Tr_{20} or Tr_{21} is in the level "1". Under this condition, the voltage V_N remains to be $5V_d$. When all the base voltages of Tr_{19}, Tr_{20} and Tr_{21} become "0" or "-1", the voltage V_N goes into V_d. In the case where the base voltage of Tr_{23}, Tr_{24} or Tr_{25} is in "1" or "0", the voltage V_O equals $3V_d$. When all the base voltages of Tr_{23}, Tr_{24} and Tr_{25} become "-1", the voltage V_O goes into V_d. Therefore T_{out} is verified to be $(p + h_1(s)).q.(r + h_{-1}(s)) + p.J_1(s) + r.J_{-1}(s)$.

The T-gate thus obtained has an ability to restore the proper voltage level for all the input of p, q, r and s. Fig. 3(a) shows a characteristic of the T-gate which is corresponding to the expansion of Eq. (1). It can clearly be seen that there exists a static hazard for the change of a control signal s. However, as shown in Fig. 3(b), the current mode circuit of the T-gate which is corresponding to the expansion of Eq. (2) is static hazard-free for the change of a control signal s.

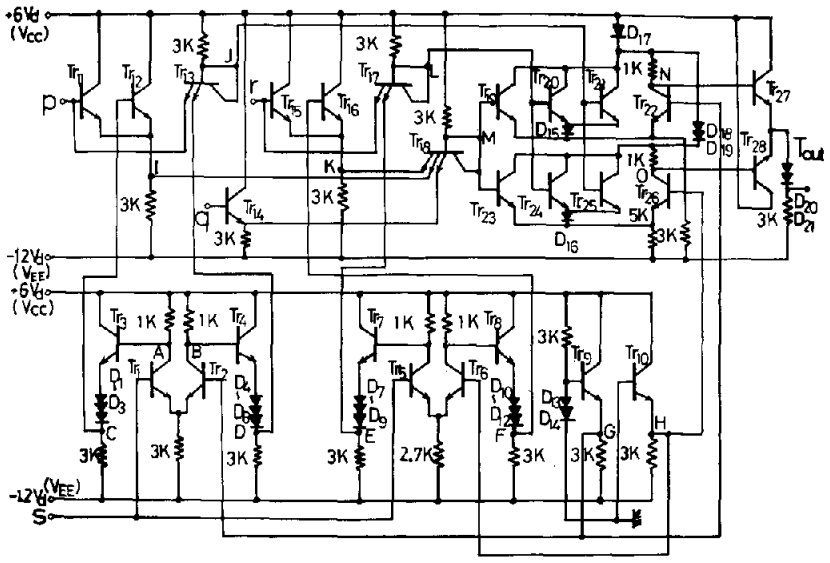
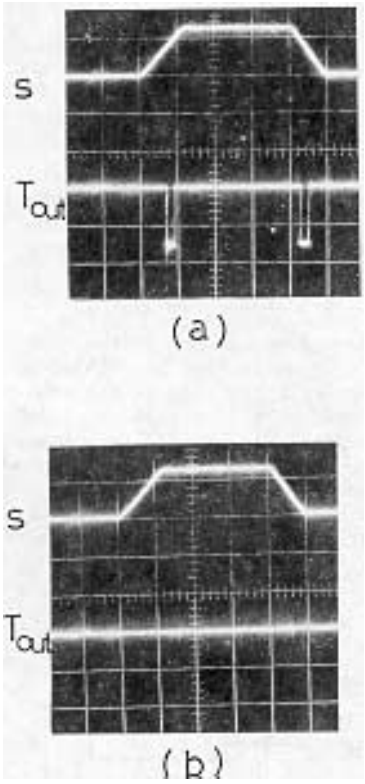


Fig. 2



20 μsec/div., 2 V/div.

Fig. 3

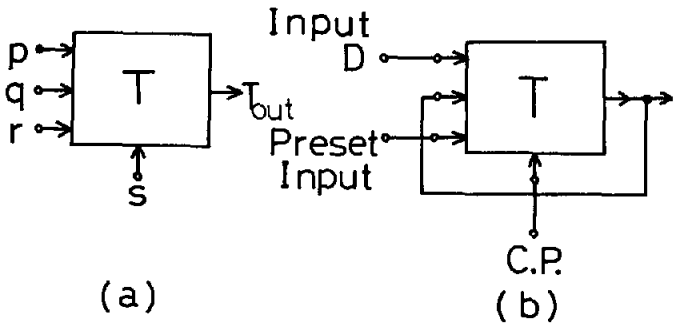


Fig. 4

III. MEMORY ELEMENTS

Ternary memory elements can easily be constructed by using the T-gates shown in Fig. 1 as building blocks. We will present several types of memory elements which are useful for constructing a ternary digital system.

1. D FFF

First we shall adopt the symbol of Fig. 4 (a) for T-gate [3]. If the clock pulse of "1" is applied to the D FFF of Fig. 4(b), then the output of D FFF, T_{out} goes into the same state as the input signal D. As soon as the clock pulse C. P. returns to "0", the input signal D will be stored with the output T_{out} fed back into the terminal q. When the negative clock pulse "-1" is applied to D FFF, the output T_{out} is put into the state at the preset input which is given as a constant value in L = { 1, 0, -1}.

Table 1 shows the excitation table of T_{out} in D FFF. For example, assume that the present state is in A and the input p is "1". First the clock pulse of "1" is applied and causes D FFF to change its state from A to B. Since B is the unstable state, it changes into stable state C immediately. When C. P. becomes "0" again,

C.P., p / q	1 1	1 0	1-1	0 1	0 0	0-1
1	(1) C	0	-1	(1) D	(1)	(1)
0	1 B	(0)	-1	(0) A	(0)	(0)
-1	1	0	(-1)	(-1)	(-1)	(-1)

(a) r:don't care

C.P., r / q	-1 1	-1 0	-1-1	0 1	0 0	0-1
1	(1)	0	-1	(1)	(1)	(1)
0	1	(0)	-1	(0)	(0)	(0)
-1	1	0	(-1)	(-1)	(-1)	(-1)

(b) p:don't care

Table 1

the state changes into the stable state D. Thus the state transition from A to D can be done, and as long as C. P. equals "0", the output T_{out} remains to be "1" regardless of the value p.

In this excitation table, the matter to be considered carefully is the transition from C. P. = 1 to C. P. = 0. In this transient time an interval when none of the signals with the same value p and q go through T_{out} must not exist. That is to say when p equals q, there must not exist the static hazard for the change of the clock pulse C. P.. As described in Theorem 2, this static-hazard-free condition is satisfied and the operation of D FFF is assured.

2. D Master Slave FFF

Two D FFFs can be combined into a D master slave FFF as shown in Fig. 5. This construction seems to be conceptually the same as the master slave FFF which is presented by Vranesic et al [8]. When the clock pulse of "1" is applied to D master slave FFF, the master responds to the input signal. The slave is disconnected from the master at this time, so the value of the output of the slave may not change while the master is responding to the input signal. Then if C. P. returns to "0", the master is disconnected from the external input signal and "1", "0" or "-1" stored by the master is transferred into the slave. In the case where C. P. of "-1" is applied, the master and the slave simultaneously respond to the preset input which is given as a constant value in L.

3. B Master Slave FFF for Bilateral Ternary Shift Register

A Bilateral master slave FFF (B master slave FFF) can be constructed by using four T-gates as shown in Fig. 6. First let us consider for the case where PE (preset enable) remains to be "0". On the arrival of the clock pulse of "1", the master responds to the shift right input (usually the output of the FFF of the previous stage). On the other hand, the clock pulse of "-1" causes the master to respond to the shift left input (usually the output of the FFF of the next stage). Thus, we can put the circuitry of left and right shifting to form a register that can shift in either direction. However, as long as PE equals "0", the FFF cannot be preset to an arbitrary initial state. The preset operation is often necessary to form a register. Let PE be "1" when C. P. equals "0". This time, the master and the slave respond to the preset input P_1. Similarly, if PE becomes "-1" during the clock pulse of "0", then the master and the slave respond to the preset input P_2. Thus the FFF can be preset to an arbitrary initial state when the clock pulse remains to be "0".

Let us now consider the necessary condition where such master slave FFF in the sequential network is well operated without misbehavior. We assume that each gate in the excitation circuit consists of T-gates, and the maximum number of stages in the T-gate network is N. Then, we must select Δ_1 and Δ_2 (Fig. 7) to satisfy

$$\Delta_1 > \Delta_T$$
$$\Delta_2 > \Delta + (N+1)\Delta_T \quad (4)$$

where Δ_T and Δ are the delay time of T-gate and G respectively.

As to the critical racing in the transient of C. P., we must consider for the inputs B and C in Fig. 7. Until the input C has completely gone to "0", the input B must not change its value. Thus,

$$\Delta_T > \Delta. \quad (5)$$

Therefore, the delay time of the gate G must be less than that of the ordinary T-gate. In order to satisfy this condition, it is better to implement the gate G as a unary function.

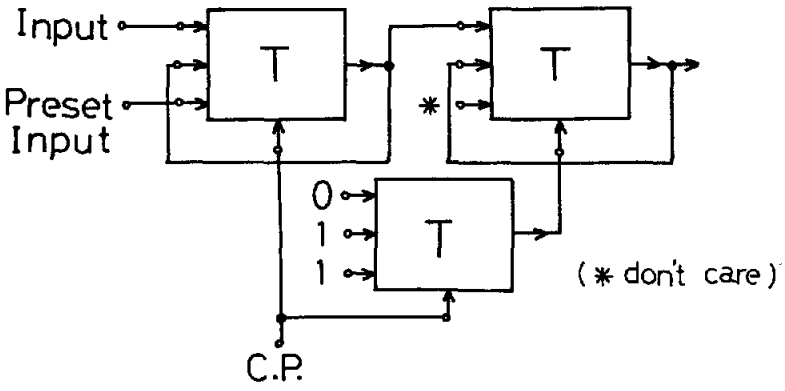


Fig. 5

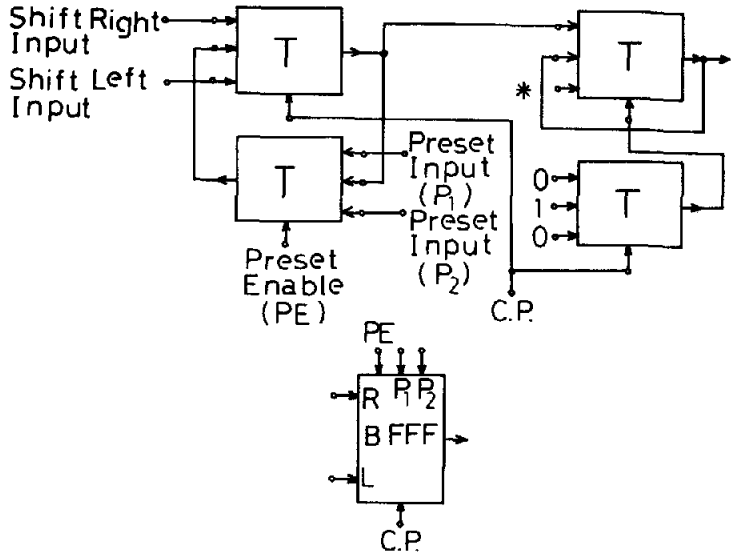


Fig. 6

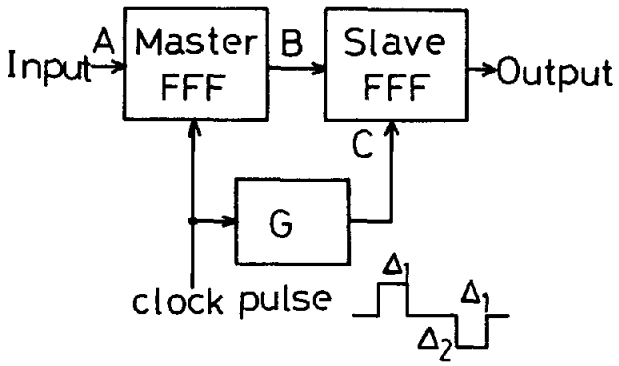


Fig. 7

Present input I	Present state S	Next state S'	Present output C
1	1	-1	1
1	0	1	0
1	-1	0	0
0	1	1	0
0	0	0	0
0	-1	-1	0
-1	1	0	0
-1	0	-1	0
-1	-1	1	-1

Table 2

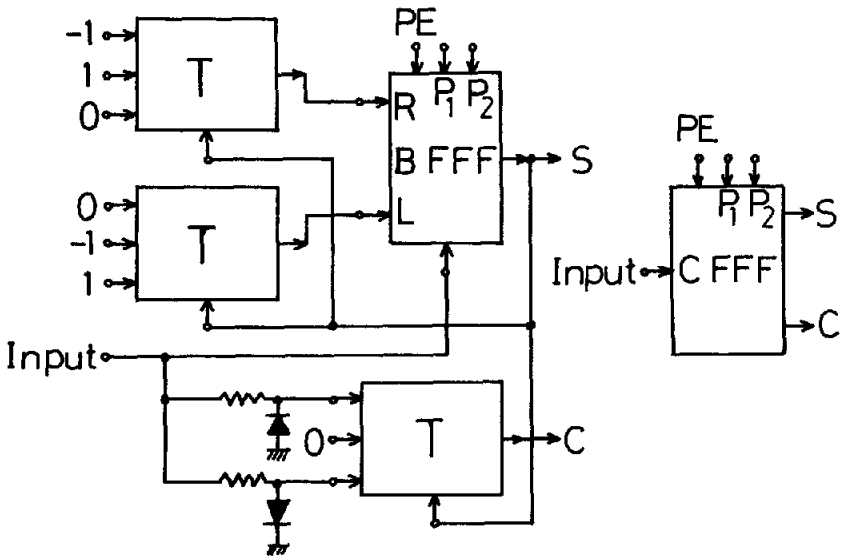


Fig. 8

4. Counting FFF

A counting FFF (C FFF) is a single-input memory element with the state transition of Table 2. The next state S' is the signed ternary sum of the present input I and the present state S. The present output C becomes the signed ternary carry of the present input I and the present state S. From this state transition table, we can write the following expression for S' and C.

$$S' = T(T(-1, 1, 0 ; S), S, T(0, -1, 1 ; S) ; I)$$
$$C = T(T(1, 0, 0 ; I), 0, T(0, 0, -1 ; I) ; S). \quad (6)$$

Fig. 8 shows that a C FFF can be realized by B master slave-construction. When the logic level "1" or "-1" is fairy greater than the level shifting voltage of diodes, then T(1, 0, 0 ; I) and T(0, 0, -1 ; I) can be replaced by simple limiter circuits using diodes and resistances.

IV. TERNARY COUNTERS

A counter is a sequential digital device that generates logic signals which can be interpreted as succesive numbers. It is essentially logic device representing numbers based on some code. There exist many number representations in the ternary logic system [7]. So, various kinds of counters which are suitable for ternary logic system must be designed.

1. Signed Ternary Counter Using C FFFs

By using C FFFs, we can realize a signed ternary counter as shown in Fig. 9, where it is assumed that the initial value placed into the C FFFs is "0" (this operation can be done when PE becomes "1"). By counting in the up direction for a positive pulse "1" and in the down direction for a negative pulse "-1", we can count both positve and negative numbers. Generally we can say that pulses up to $\pm (3^N-1)/2$ can be counted by N stages of C FFFs. The counted result is represented by $\sum_{i=0}^{N-1} S_i \cdot 3^i$, where S_i denotes the state of

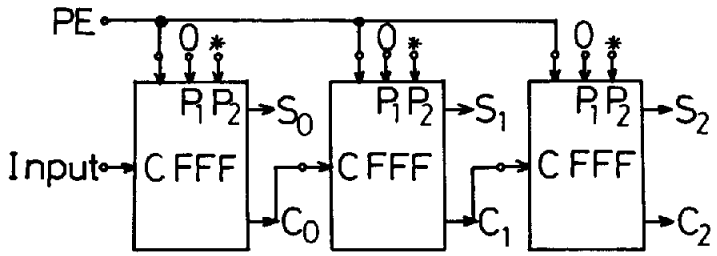
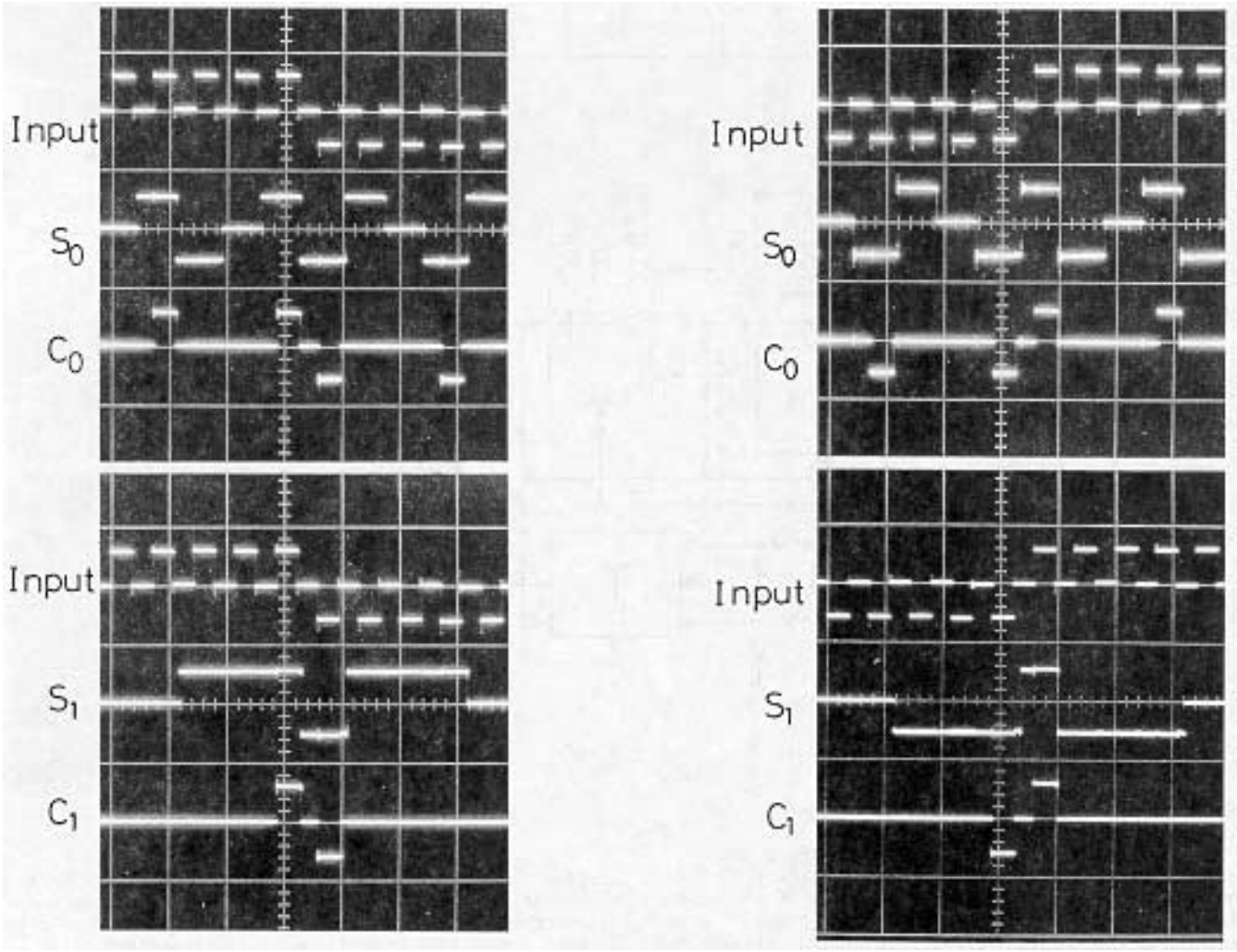


Fig. 9



50 μsec/div., 5 V/div.

Fig. 10

50 μsec/div., 5 V/div.

Fig. 11

the i+1-th C FFF from the left-hand end.

Although the signed ternary counter gives the greatest efficiency of number representation, it requires the most decoding logic and gives the greatest ripple effect similar to the binary asynchronous counter. The practical operating waveforms of a signed ternary counter are obtained in Figs. 10 and 11 by using a four channel synchroscope.

2. Shift Register Counters

(1) One-of-N

A one-of-N, or ring counter consists of N stages of B master slave FFFs operating such that one and only one of FFFs is "1" or "-1" at a particular time. Fig. 12 shows a one-of-N counter with three stages of B master slave FFFs. It consists of a recirculating shift register with its output connected to its input with ternary negation [1]. This counter with N stages can represent 2N values. For example, such a counter

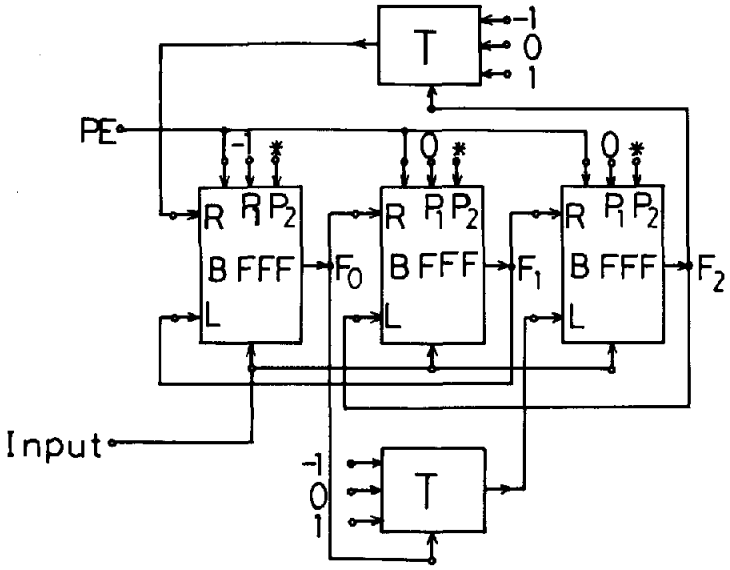
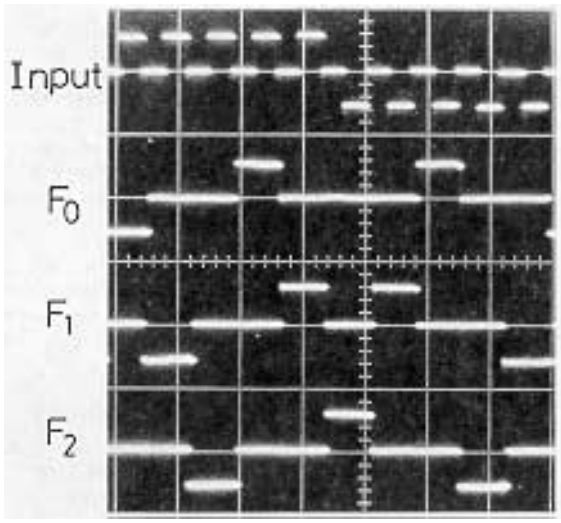


Fig. 12



50 μsec/div., 5 V/div.

Fig. 13

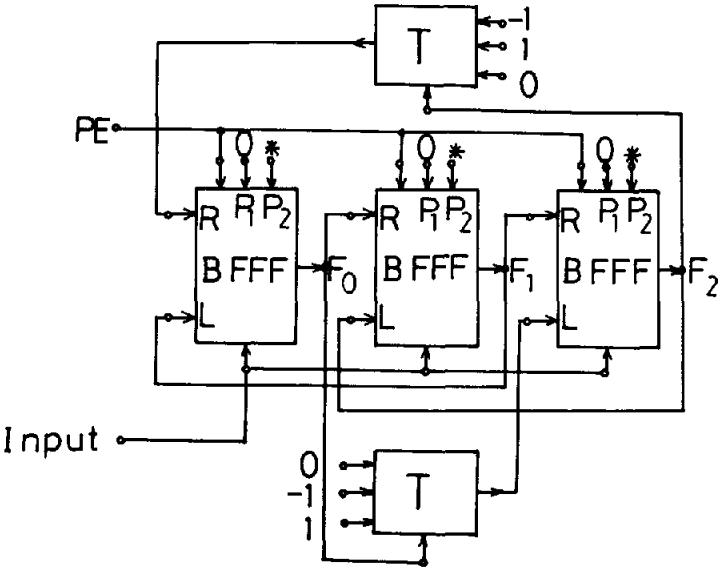
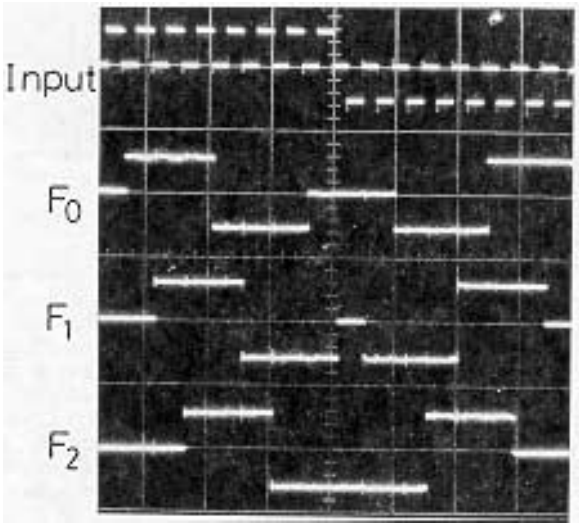


Fig. 14



50 μsec/div., 5 V/div.

Fig. 15

Count	F_0	F_1	F_2
0	-1	0	0
1	0	-1	0
2	0	0	-1
3	1	0	0
4	0	1	0
5	0	0	1

Table 3

Count	F_0	F_1	F_2
0	0	0	0
1	1	0	0
2	1	1	0
3	1	1	1
4	-1	1	1
5	-1	-1	1
6	-1	-1	-1
7	0	-1	-1
8	0	0	-1

Table 4

with N = 3 will have the sequence as shown in Table 3.

Before starting to count, only the left-hand end FFF of the register is preset to "-1", and the other FFFs are preset to "0". Each time the counting pulse becomes "1", this "-1" or "1" is shifted to the right. As to down counting, this "-1" or "1" is shifted to the left, so that the left-hand end FFF of the register is connected to the right end FFF of the register with ternary negation. These practical operating waveforms are shown in Fig. 13.

The advantage of a one-of-N counter is that it does not require decoding in order to obtain seperate signal outputs for each number. The decoding output for the count n is given as F_n (mod N). It is possible to use this as a ternary multiplexer switch.

(2) Switch ring counter

When the right shift is done, then the output of the rightmost FFF is connected to the input of the leftmost FFF through a cycling [1] gate. When the left shift is done, then the output of the leftmost FFF is connected back to the rightmost FFF through a double-cycling [1] gate. Thus, we can realize a switch ring counter as shown in Fig. 14. The sequence will proceed as in Table 4. By starting with the FFFs cleared to "0", this counter with N stages can represent 3N values. These practical operating waveforms are shown in Fig. 15.

It is three-halves as efficient as the one-of-N counter, however, decoding is required to obtain a seperate logic output for each value. But, the decoding is simple because only a two input ternary function is required for each. The decoding inputs for the count n are given as F_{n-1} and F_n (mod N).

V. CONCLUSION

We have presented the theoretical and experimental considerations for the ternary T-gate as a static-hazard-free memory element. These memory elements are operated with the ternary clock pulse, which leads to the reduction of the number of input and output terminals. The ternary counters realized using T-gates are superior to the binary one in that the up-down counting can easily be carried out by only one input signal. The ternary logic system can be constructed by using such T-gates as basic building blocks. It is expected that the T-gates are applied to ternary sequence generators, arithmetic calculators, etc..

The T-gate network will be important with the potentialities of the integrated circuit. Therefore, the development of the circuit aspects with high speed and reliability will be hoped for in the future. However, a number of transistors are required to realize a ternary digital system using T-gates. Though this matter is a disadvantage from the point of view of the density of integration, the concept of T-gate is very useful for the notation of a logical function and simplifies the synthesis problem.

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