A TERNARY J – K MEMORY *

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Abstract : A description of a ternay J – K type flip – flop is presented . The output is in the form of three valued level 2, 1, 0 . The circuit may be set to any logic level as well as retain the present , past and former past information in accordance to a defined J – K input logic level . This type of triflops have been selected in order to have flexible to ternary memory with simple excitation equations .

1. Introduction

Recent articles has shown much interest in the theory and design of multivalued (m.v.) memory circuits[1–6] . Many approaches and different realisation schemes have been suggested . The excitation equations of binary D, T, R – S and J – K flip – flops are used in the design of the multi – stable types. . The description of a 3 valued memory elements is found in the literature 3,4,5 .

Ternary means an element of a switching which will perform 3 – valued transmission and 3 valued switching . A 3 valued variable 'Q' will assume three values Q , $\bar{Q}$, and $\bar{\bar{Q}}$, where the bar sign signifies cycling . Some authors such as Yofli and Rosenfeld and Porat[7] have suggested (2,1,0) as the logic states for a ternary variable . This paper describes a J – K tristable with analogy to the binary system memory J – K flip – flop . Integrated circuits , a few external resistors and transistors are used throughout .

2 Basic Circuit Design

The basic circuit design relies on the implementatiion of translating circuits between the ternary and binary set . Ternary output is obtained with the aid of a combining circuit . The logic states are represented by voltage levels as given below :

2 ≡ $\geqslant$ 3 volt

1 ≡ 3 volt $\geqslant$ v $\geqslant$ 1.5 volt

0 ≡ $\leqslant$ 1.5 volt

It was required that the J – K tristable should have the following :

(a) J – K data input .

(b) Clocked input .

(c) Preset inputs , SET 0 , SET 1 , SET 2 ,

(d) Retain present , past or former past information in accordance to a defined J – K input data .

Recently some of the authors such as Acha and Heurtas[1] have defined the concept of JK m.v . memory element and have discussed the advantages of this flip – flop . For ternary systems the JK flip – flop is defined as follows : a JK 3 valued flip – flop is one which has at least one 3 valued output and three valued inputs (J0 , J1 , J2) with the excitation table which is shown in Table 1 .

As can be seen from Table 1 , the input Jm has to be n if a transition from state m to state n must occur . It is not necessary to specify more than one input at a time .

Table 1 JK triflop excitation table

y	y^+	J0	J1	J2
0	0	0	x	x
0	1	1	x	x
0	2	2	x	x
1	0	x	0	x
1	1	x	1	x
1	2	x	2	x
2	0	x	x	0
2	1	x	x	1
2	2	x	x	2

This paper describes a J – K triflop whose excitation table is shown in table 2 which gives the logical operation behind this type of ternary memory .

Table 2 : Ternary J – K memory truth table

Input data		Output
J	K	Q_{n+1}
0	0	Q_n
1	0	1
2	0	0
0	1	1
1	1	$\bar{Q}_n$
2	1	2
0	2	0
1	2	2
2	2	$\bar{\bar{Q}}_n$

where Q_n and Q_{n+1} are the present and next states respectively . Table 2 has been arranged in analogical manner to the J – K binary flip – flop truth table . For example , when JK = 00 , the next state will be as that of the present one. Instead , for JK = 11 , it will be the complement or the cyclic shift of the present state . Similarly , for JK = 22 , a double cycling is achieved for the next transition . The combination of JK = 02 or 20 will give 0 as the next state , while for JK = 01 or 10 it will be 1; and for JK = 12 or 21 , Q_{n+1} will be at logic 2 .

3 Practical Realisation

There are three outputs represented by Q , $\bar{Q}$, and $\bar{\bar{Q}}$; where :

$\bar{Q} = Q + 1$

$\bar{\bar{Q}} = \bar{Q} + 1$

i .e. the three outputs are in cyclic shift mode to one another . Fig. 1 shows the basic building blocks of the J – K ternary memory . It consists of six stages : (1) Input decode (2) Input logic (3) Storage (4) Set logic (5) Output logic (6) Output encode .

3.1 Input Decode

This is achieved by means of two analog comparators (uA 710) for each input data (J or K) and in accordance to table 3 and Fig. 2 .

Table 3 Input decode table

J (or K)	a	b	J (or K)	a
0	0	0	0	0
1	1	0	1	1
2	1	1	2	x

where x denotes don't care condition .

3.2 Storage

The storage is achieved by means of two D – type flip – flops , two being the minimum number required to store the information presented to them by the input decoding circuit .

3.3 Preset Facilities

It was required to have preset facilities that will enable the Q output to take on the logical value 0 , 1 , or 2 in accordance to a single pulse application at the S_0 , S_1 or S_2 terminals respectively . The $\bar{Q}$ and $\bar{\bar{Q}}$ outputs remaining in cyclic shift mode with the Q output . The preset inputs for the tristable are denoted as S_0 , S_1 , and S_2 while the set and reset inputs to the two D flip – flops are denoted as S_C , R_C , S_D and and R_D . Following the preset truth table shown in table 4 below ,

Table 4 Preset truth table

Preset	C	D
S_0	0	1
S_1	1	0
S_2	0	0

We can write the following logical relationship :

$S_0 = R_C \cdot S_D$

$S_1 = S_C \cdot R_D$

$S_2 = R_C \cdot R_D$

Hence :

$S_C = S_1$

$R_C = S_0 \cdot S_2$

$S_D = S_0$

$R_D = S_1 \cdot S_2$

from which the preset logic is shown in fig. (3).

3.4 Output Encode

The D type flip - flops binary outputs are shown in the truth table (table 5) .

Table 5 Storage truth table

Logic level	C	D	E	F	G	H
0	x	1	1	0	0	0
1	1	0	0	0	x	1
2	0	0	x	1	1	0

There are at the output encoder section three circuits fo the same components that translate binary data into ternary one . These circuits recieve from the output logic six inputs C , D , E , F , C , and H which are fed to output encode circuitries . Fig. 4 shows the complete schematic diagram for the ternary J - K memory employing TTL gates .

4 Practical Results

The J - K triflop described above have been constructed and tested . Fig . 5 shows the output and input clock waveforms of a modulus - 3 counter for clockfrequencies of 10 KHz and 1 MHz respectively .

5 Conclusions

The use of TTL and integrated circuits in the realisation of 3 - valued J - K memory elements has been discussed . The design of variety control input ternary memory is implemented .

Practical results are given that shows much interest in the versatility and speed of the implementation which have been studied . Irving et al[4] have pointed out that m.v. logic circuits may increase their interest in the future because they allow an increase of the information content per signal line . That means a reduction of the number of interconnections . This will have the advantages of lowercost , better reliability due to lower number of interconnections and higher speed .

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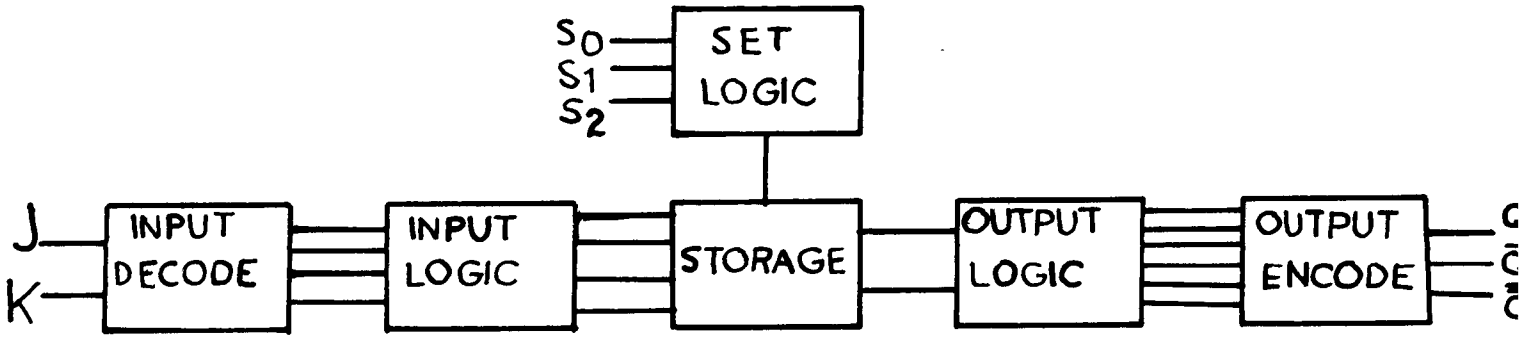
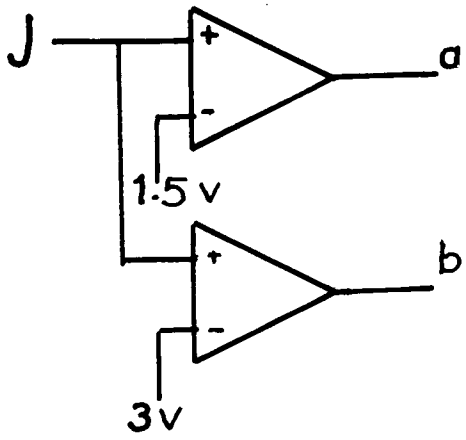


FIG1 BLOCK DIAGRAM OF THE JK TRISTABLE



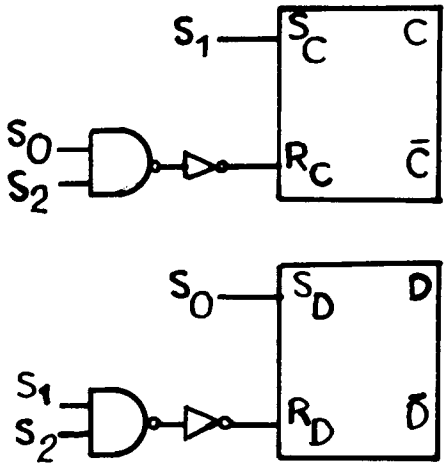


FIG 2 INPUT DECODING CIRCUIT FIG3 SET LOGIC FOR THE JK TRISTABL

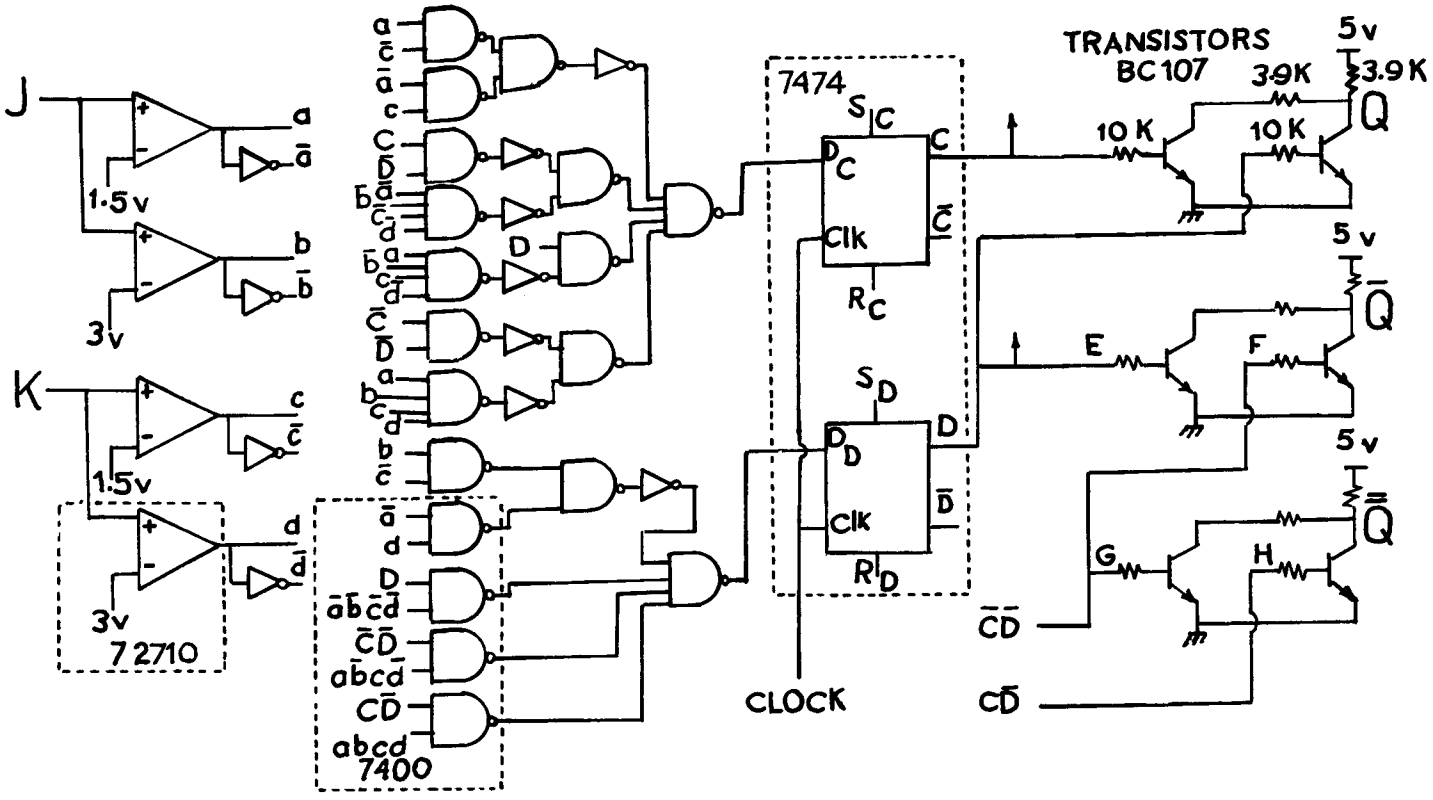


FIG 4 SCHEMATIC DIAGRAM OF A TERNARY JK MEMORY EMPLOYING TTL GATES

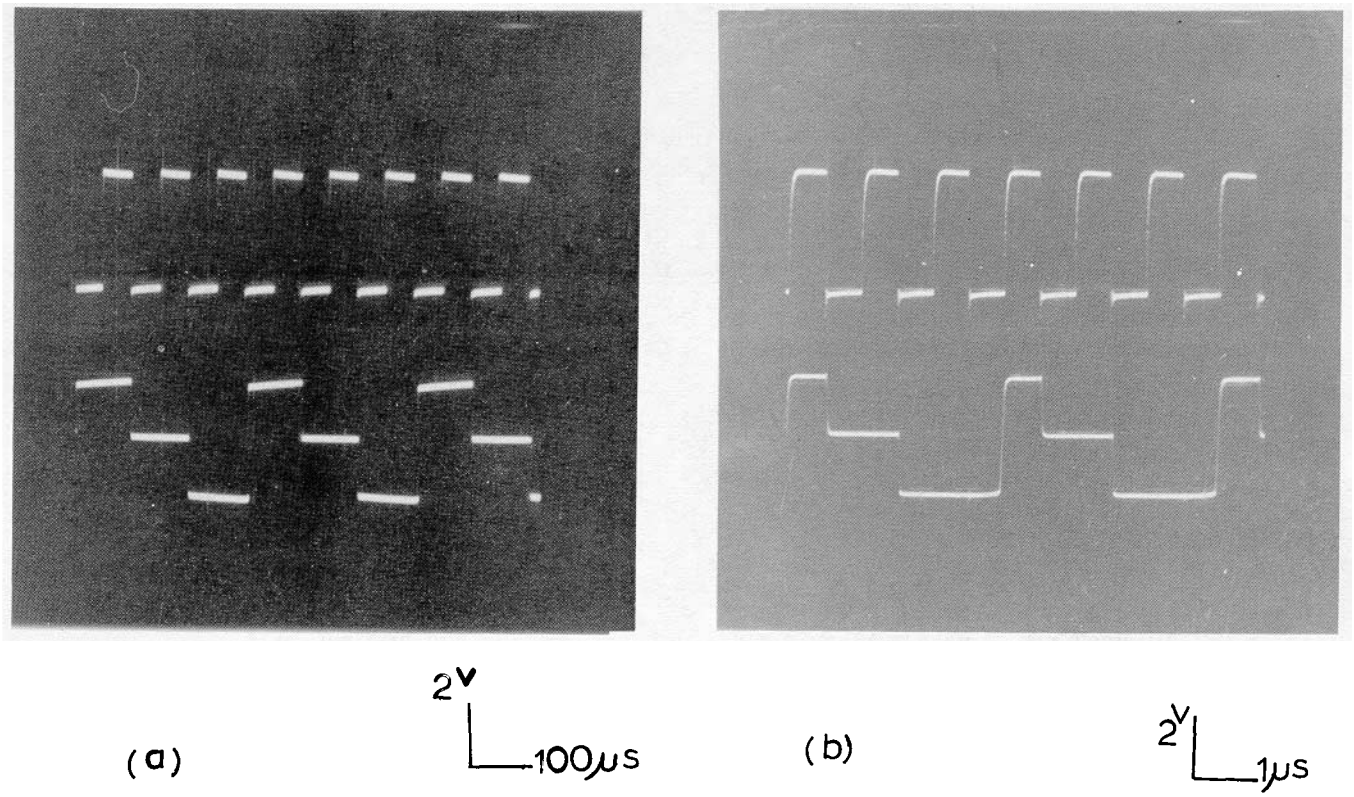


FIG 5 CLOCK AND OUTPUT WAVEFORMS OF THE JK TRISTABLE WITH A CLOCK FREQUENCY OF (a) 10 KHZ (b) 1 MHZ