# A SIMULATANEOUS ANALOG / TERNARY CONVERTER

M. A. H . Abdul – Karim and N. E. Berbat *

* Department of Electrical Engineering , College of Engineering ,
University of Baghdad , Baghdad , IRAQ .

This note presents a technique of designing 2 bit simultaneous analog to ternary convertor with 100 ns response time . TTL logic components were used throughout the prototype design .

## 1 Introduction :

Recent technical work have shown some advantages of using multi – valued logic where the natural question was if there is a practical radix other than 2 that will produce circuits with greater saving in components , without loss of speed . Alexander (1964) showed that the most efficient radix for implementation of switching systems is the natural base (e = 2.71828) , it seems likely that the best integral radix is 3 rather than 2 . Ternary gives the meaning of a switching system which will perform 3 – valued transmission and 3 valued switching . A ternary variable Q will assume three values Q , $\bar{Q}$ , $\bar{\bar{Q}}$ , where the dash sign means cycling . This note deals with a circuitry which is able to perform a 2 bit A/T conversion that may be used as part of a instrumentation system , for example .

## 2 Circuit Working Principle

Figure –1– shows the block diagram of A/T convertor , and table –1 – gives truth table for this circuit .

Three distinct sections can be identified . The first is comprised of $3^n - 1$ analog comparators yielding $3^n - 1$ parallel signals . The second one is the binary encoder logic circuit which produces from $3^n - 1$ binary inputs 2n binary outputs . The third section is a transistor circuits designed to translate the binary outputs into ternary form . The logic states are represented by voltage levels as given below .

2 ≡ 3 volt ⩾ v ⩾ 1.5 volt

1 ≡ ⩾ 3 volt

0 ≡ ⩽ 1.5 volt

Table 1

| $V_{in}$ | Ternary o/p | |
|---|---|---|
| | $x = 3^0$ | $y = 3^1$ |
| 0 | 0 | 0 |
| 1 | 1 | 0 |
| 2 | 2 | 0 |
| 3 | 0 | 1 |
| 4 | 1 | 1 |
| 5 | 2 | 1 |
| 6 | 0 | 2 |
| 7 | 1 | 2 |
| 8 | 2 | 2 |

Figure –2– illustrates a parallel 2 – bit A/T convertor which has been constructed and tested . It employs commercially available integrated circuits and discrete components throughout . The outputs of the comparators A , B , C , D , E , F , G and H are either at logic "0" or logic "1" , and they are fed to the binary encoder logic circuit as shown in table –2– .

Table 2

| $V_{in}$ | Comparator Output | | | | | | | | Encoder Logic o/p | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Volts | A | B | C | D | E | F | G | H | S | T | U | V |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0.5 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1.5 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 2 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2.5 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 3 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 3.5 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 4 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |

The four binary encoder outputs S , T , U and V are also at either logic '0' or logic '1' and are applied to their respective output transistor circuit . The binary input data are translated into ternary form by means of the binary / ternary convertor circuit . This translating circuit is comprised of four transistors for a two bit ATC . When S and T are low , the output X will be at logic 1 , i.e . X ≡ 1 , but when S is high and T is low , X ≡ 2 , nowever if S is low and T is high , X ≡ 0 as was defined before . The same reasoning applies for ternary output Y in terms of binary inputs U and V as shown in table -3- .

| $V_{in}$ | Encoder Logic Output | | | | Ternary o/p | |
|---|---|---|---|---|---|---|
| Volts | S | T | U | V | X | y |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0.5 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 2 | 0 |
| 1.5 | 0 | 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 0 | 0 | 1 | 1 |
| 2.5 | 1 | 0 | 0 | 0 | 2 | 1 |
| 3 | 0 | 1 | 1 | 0 | 0 | 2 |
| 3.5 | 0 | 0 | 1 | 0 | 1 | 2 |
| 4 | 1 | 0 | 1 | 0 | 2 | 2 |

Table – 3 –

The response time is determined by the input to output transfer delay of the comparators plus the worst case propagation delay through the binary encoder and the output transistor circuit . The comparators have a response time of around 40 ns . The binary encoder is comprised of three parts of 7400 series TTL logic ; this and the translating binary / ternary transistor circuit will give together a propagation delay of around 60 ns . Thus the A/T convertor has a response time of around 100 ns , this may be improved by using higher speed components .
The problem of the exponential increase , $O(3)^n$ in the necessary number of devices remains . Thus the complexity of simultaneous convertors is unavoidable .

References :


1. Alexander W. Feb . 1964 Electronics and Power 36 .
2. Contoni A. July 1973 Proc . of IREE , 230 .
3. Yoeli M . and Halpern I . 1968 Proc. IEE , 115 , 10 .

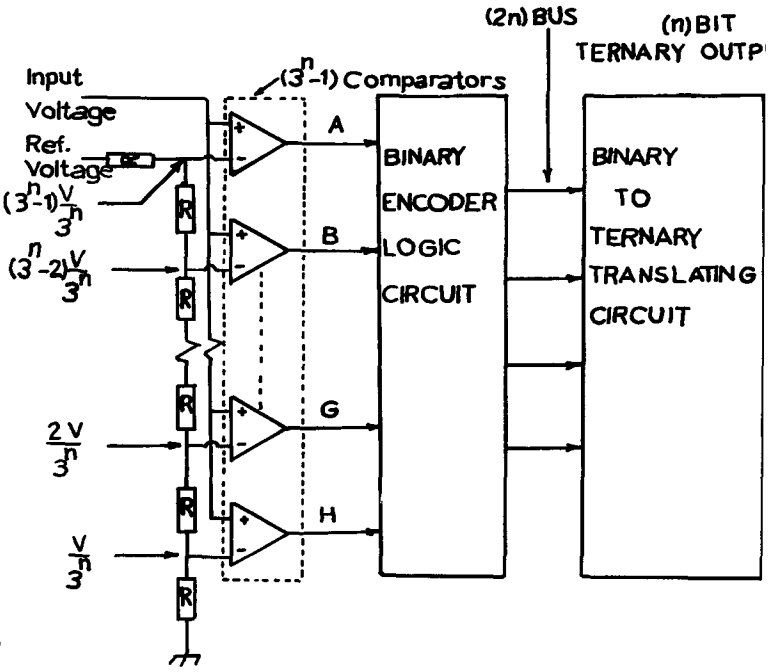




FIG1 Block Diagram of Simultaneous Analog-To-Ternary Converter

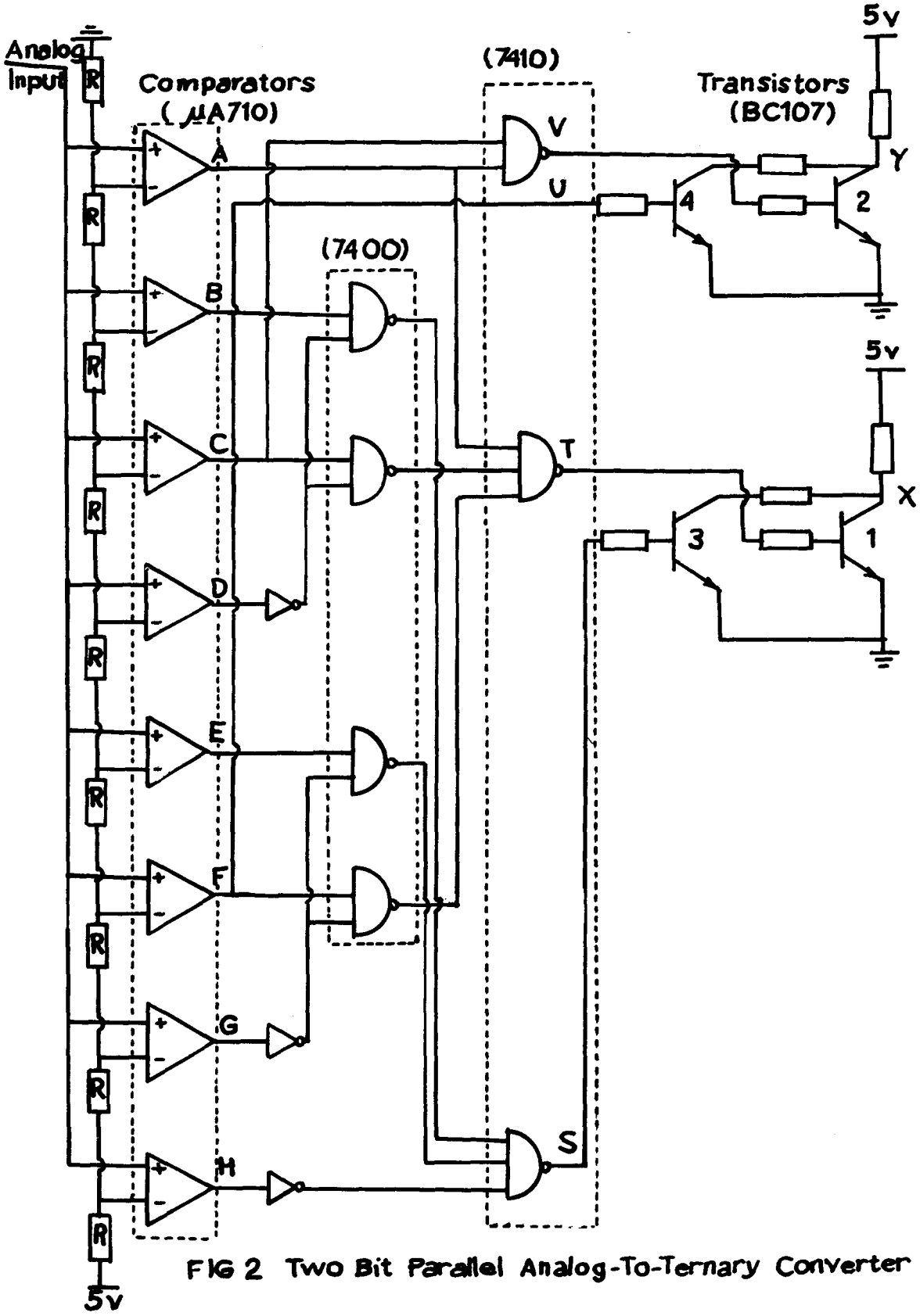



FIG 2 Two Bit Parallel Analog-To-Ternary Converter